Endorsed by

300 mm Photonics

White Paper

authored by Photonics21

and endorsed by the Association for European NanoElectronics Activities *AENEAS*

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Some photonic products and technologies will very soon need to transition to 300 mm wafers for reasons such as performance, cost, and capacity. Without these transitions, European industry and society risk becoming dependent on US and/or Asian suppliers. This white paper identifies the products and technologies that are ready for and in need of transition: micro-bolometer imagers, Photonic Integrated Circuits (PICs), and the 300 mm epitaxy and wafer-level test tools needed to manufacture them. The white paper also evaluates what is at stake.

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1. Abstract

Some photonic products and technologies will very soon need to transition to 300 mm wafers for reasons such as performance, cost, and capacity. Without these transitions, European industry and society risk becoming dependent on US and/or Asian suppliers. This white paper identifies the products and technologies that are ready for the transition, including micro-bolometer imagers, Photonic Integrated Circuits (PICs), and the 300 mm epitaxy and wafer-level test tools essential for their production. It also examines what is truly at stake:

- **Sales: by 2028/2029, € 1.8 billion of annual sales of micro-bolometer imagers, PICs and 300 mm photonics tools by European companies**
- **Jobs: by 2028/2029, 7300 direct jobs in Europe in the sectors of micro-bolometer imagers, PICs and 300 mm photonics tools**
- **European sovereignty in dual use and critical technologies**

These transitions will position Europe as a leader in the photonics industry, being at the forefront of the move toward larger 300mm wafers. Anticipating this transition will help build a sovereign European market. This transition will require expensive developments and will not be possible without the support of the European Commission and the Member States. Photonics21 solicits support for the R&D phase through Chips JU dedicated funding and through facilitated access to 300 mm pilot lines whenever possible, as well as the activation of the First-of-a-Kind mechanism of Chips Act Pillar II if no industrial facility in Europe is able to ensure manufacturing on 300 mm wafers.

2. 300 mm, a Necessary Transition for European Photonics Industry Competitiveness

The European Chips Act is the European Commission's response to the awareness of semiconductor chips' strategic nature. Pillar I of the Chips Act establishes the Chips for Europe Initiative with the Chips JU as its main implementer. One of its objectives is to enhance existing and develop new advanced pilot lines. As of today (September 2024), the Chips JU has published five new pilot line calls. Three of them are dedicated to purely electronic components: advanced 2 nm nodes, 7 nm nodes on fully depleted silicon-on-insulator and devices based on wide band gap materials. One is dedicated to developments in Photonic Integrated Circuits (PIC). One is dedicated to advanced packaging and heterogeneous integration, which involves combining chips from different domains: logic, memory, sensing, RF and communication, and photonics.

Even though photonics is present and the packaging pilot line should address the 200 mm and 300 mm wafer platforms, overall, there is still a strong focus on More-Moore technologies on 300 mm wafers.

The risk is that the technology gap between 200 mm and 300 mm Si technologies amplifies. Today, 300 mm Si technologies offer capabilities that 200 mm technologies do not have:

- Photolithography tools with the most advanced immersion systems and Extreme UV sources
- CMOS Technology nodes below 90 nm
- Most advanced 3D wafer stacking using hybrid bonding technologies thanks to memory on logic and logic on logic Systems on Chip (SoC) based on advanced nodes only available on 300 mm wafers

Without these capabilities, some photonics products/technologies based on 200 mm wafer processing are at risk of being limited in terms of performance, cost and capacity and not being able to satisfy the market requirements and demands. The products and technologies the most in need of the 300 mm capabilities are PICs and infrared thermal imaging sensors. These products/technologies are described in §6.1 of ANNEX A1 and §7.1 of ANNEX A2. Specific semiconductor tools necessary to manufacture photonics products on 300 mm wafers will also need to be developed.

These are identified in the introductory part of §8 (ANNEX A3). Epitaxy and Wafer Level Testing are described in §8.1 and §8.2.

For the progress brought by the Chips Act to the semiconductor industry to diffuse ultimately to the Photonics products in need of advanced performance, lower cost or higher capacity, it is necessary to ensure that these products and semiconductor tools start transitioning to 300 mm wafers. The key motivations for these products to transition to 300 mm are described in §6.4 of ANNEX A1 and §7.4 of ANNEX A2.

The cost of developing processes and products on 300mm wafers is significantly higher than on 200mm wafers, especially because of the high mask-set costs. Unless Multi Project Wafers (MPW) can be used extensively, the development costs of photonics products and technologies on 300 mm wafers will be expensive. It is, unfortunately, not always possible. Moreover, it will be necessary in some cases to develop and/or invest in semiconductor process tools compatible with 300 mm wafers. This will be difficult for small, medium, and intermediate-sized companies, which are the core of Europe's photonics industry. These developments and investments need to be supported to secure Europe's competitiveness and sovereignty.

Different types of European R&D and investment support mechanisms are available. Among them are Important Project of Common European Interest (IPCEI), First-of-a-Kind (FoaK), Innovation Actions under the Chips JU, as well as loans and equity funding from the European Investment Bank (EIB), the European Innovation Council (EIC) Accelerator, and initiatives like the Strategic Technology European Platform (STEP) programme. Among these possibilities, the right choice will depend on the specificities of each technology, product type, development stage, nature of the action to be supported and ecosystem funding situation:

- For microbolometer imagers, defining the most competitive option to satisfy the automotive market needs in terms of performance versus cost trade-off still needs to be settled. It will require extensive developments on 300 mm wafers that may not be compatible with MPW because of the set of materials necessary for the micro-bolometer process. It may also require the development of specific 300 mm tools for these materials. These developments will need support.
- For Photonic Integrated Circuits (PICs), the opening of a Chips JU call for a Pilot Line will provide support for the development of the silicon-based part of PICs on 300 mm wafers as well as support for the development of heterogeneous integration of sub-parts of the PICS (lasers...) on silicon and packaging. The development on 300 mm wafers of the other materials required for advanced PICs may come second in the priority list of the pilot line. The development of the 300 mm tools and processes for these materials, namely Silicon Nitride, Barium Titanate (BTO), Lithium Niobate, and III-V epitaxial structures, will need support.

Based on these considerations, today, Photonics21 identifies Chips JU dedicated funding as a relevant support mechanism. It thus solicits support for the R&D phase through this mechanism, as well as facilitating access to 300 mm pilot lines whenever possible.

The first industrial deployment of the photonics products of interest described here may also require heavy investments to establish the manufacturing capabilities that will ensure the 20% market share goal of the European Chips Act. Photonics21 wishes to alert the European Commission and Members States of the potential need to activate the First-of-a-Kind mechanism of Chips Act Pillar II for this phase if no industrial facility in Europe is able to ensure manufacturing.

3. Impact on European Industry

Without this transition, the European Photonics industry would be limited in terms of Performance, Product cost, Capacity, and Sovereignty in both large-volume markets (automotive, consumer electronics...) and critical/strategic

low-volume markets (security, surveillance, defence…). The applications and markets that can be served by products/technologies on 300 mm wafers are described in detail in §6.2, §6.3 and §6.5 of ANNEX A1 and §7.2, §7.3 and §7.5 of ANNEX A2. For tools requiring developments to process 300 mm wafers, the types of products requiring these tools are reminded in §8. The market key drivers and trends for epitaxy tools are described in §8.1.3 and §8.1.4 and for Wafer Level Test in §8.2.3 and in §8.2.4 of ANNEX A3.

Without this transition, Europe would miss significant sales and job creation opportunities. These are detailed in §6.6, §7.6 and §8.3 of ANNEXES A1, A2 and A3. For 2028/2029, consolidating the sales and job numbers computed with a 20% market share for Europe, as ambitioned by the Chips Act, yields:

Sales: € 1.8 billion in sales of micro-bolometer imagers, PICs and 300 mm photonics tools by European companies

Jobs: 7300 direct jobs in Europe in the sectors of micro-bolometer imagers, PICs and 300 mm photonics tools

The supply chains of these industries would also risk disruption by geopolitical events and/or major international disruptions like pandemics. The semiconductor crunch that followed the COVID pandemic had a major disruptive effect on the European automotive sector. A study by Allianz (Missing chips cost €100Bn to the European auto sector[1]) estimates that the semiconductor crunch cost Europe around €100bn over 2021 and 2022. In the electronic components list for automotive, more and more photonics components are present, such as flat panel displays, smart lighting, LIDAR, visible and infrared imagers, and in-cabin monitoring. This clearly demonstrates the strong dependency of this key European industry on the reliability of the electronic and photonics supply chain.

Moreover, some types of photonics products are used in both large-volume markets and niche markets, such as safety, security, space, and defence. For example, infrared thermal imagers are used both in the automotive sector and for night vision in the safety, security, and defence sectors. For these dual-use products, 300 mm technologies bring cost and capacity advantages for large volume markets and high product performance for Safety, Security, Space and Defence niche markets. Developing and deploying 300 mm capabilities for these product types is key for both the European industry and economy and for its sovereignty in critical sectors such as Safety, Security, Space and Defence.

4. Supporting Evidence

The Chips JU call Chips-2024-CPL-5[2] intends to establish a Pilot Line on Advanced Photonic Integrated Circuits (PICs) focusing on advancing PIC technologies beyond the current state-of-the-art. Two of the expected outcomes resonate with the topic of this white paper:

- "Develop scalable and cost-effective manufacturing processes for PICs, ensuring **compatibility with current industrial standards** and promoting widespread adoption". Industrial standards are currently split on both 200 mm and 300 mm wafers but will transition more heavily in the future to 300 mm.
- "Foster the **integration of PICs with electronic integrated circuits, enhancing the functionality and efficiency of combined systems** for applications in computing, telecommunications, and beyond". The most advanced functionalities require advanced nodes that are only available on 300 mm wafers.

[1] https://www.allianz-trade.com/content/dam/onemarketing/aztrade/allianz-trade_com/en_gl/erd/publications/the-watch/2022_09_13_European-Auto.pdf

[2] https://www.chips-ju.europa.eu/File/download.aspx?entity=crf98_callfiles&attribute=crf98_file&ID=ad20f0af-3f48-ef11-bfe2-000d3ab8107a

It is thus logical to see these expected outcomes expressed in the following expected result of the pilot line: "**Extended capabilities of current PIC technologies to larger wafer sizes** and integrate built-in self-test methodologies, enhancing the performance and integration of PIC modules."

Although the Pilot Line funding will allow for some process developments on 300 mm, as explained in §2, it will not be able to cover all the materials for advanced PICs. Moreover, it will also not be sufficient to establish European manufacturing capabilities aligned with the Chips Act ambition of a 20% market share.

Concerning micro-bolometer imagers, in its 2022 report "Thermal Imaging and Sensing 2022 - Market and Technology Trends 2022", Yole Group already identified a possible need to switch from 8'' (200 mm) to 12'' (300 mm) around 2027. This appears in the Yole Group roadmap at the same time as 10 µm and lower pixel pitch thermal imagers are expected. 300 mm CMOS nodes will indeed be needed to decrease pixel pitch and, at the same time, increase imager functionalities (see § 6.4).

Furthermore, in the OPTRO conference 2024 paper "A Discussion Regarding the Supply Chain for Infrared Imaging Systems" by J.G. Zeibel from US Army C5ISR (The Centre for Command, Control, Communications, Computers, Cyber, Intelligence, Surveillance and Reconnaissance), the author mentions that "Most of the readout circuitry that is mated to thermal imaging focal plane arrays is based on twenty-year-old silicon foundry processes. (...) However, a number of upcoming transitions have the potential for significant market impacts. Some transitions may reduce production costs significantly, such as moving from 200mm wafers to 300mm wafers. Others have the potential to provide new capabilities, such as integrated photonics or 3-D stacking. But, each of these changes will require significant non-recoverable expenses that must be funded from somewhere in order to be folded into the infrared imaging supply chain. The choice to not make these changes will eventually be corporate non-viability". The analysis clearly expresses the inevitable need to transition to 300 mm for defence applications. Considering the small volumes that defence applications represent, it can only happen at the same time as the transition of large-volume products.

Now, looking at the global Photonics market, Tematys Photonics 2024 Market Study[3] shows (Figure 1) that Europe's market share has slightly declined from 2005 to 2022 (19% to 15%) along with a huge growth for China (10% to 32%).

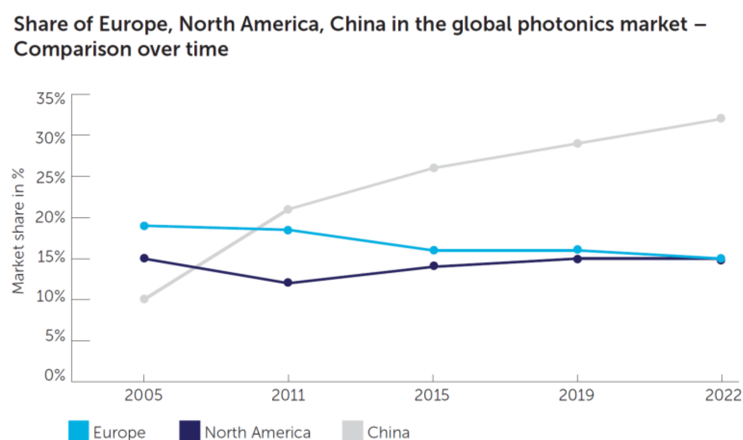


Figure 1: Evolution over time of the share of Europe, North America and China in the global photonics market Source: Tematys/Photonics21, 2023.

The products and technologies considered in this white paper, imagers, PICs, and 300 mm tools, belong essentially to the "Photonics components and materials" segment.

[3] Market_Research_Study_Photonics_2024.pdf (photonics21.org)

Photonics components and materials are the building blocks of all photonics systems. In 2022, this segment generated €21 billion in Europe [3]. In particular, the imagers, PICs and 300 mm tools of concern in this white paper are used in the following Photonics market segments (see Tematys Photonics 2024 Market Study for the complete segmentation of Photonics applications):

- Mobility: LIDAR, Cameras, speed and distance optical sensors
- Industry 4.0: Process Spectroscopy, Gas sensing, Non-conventional imaging systems
- Telecommunication and quantum information: Telecom Devices (QC, Tx/Rx, TOSA...)
- Defence & Security: Night vision, Camera for security & video-surveillance
- Large instruments and space: Components and Systems
- Instrumentation and Optical Measurements: LIDAR, Spectroscopy, other sensors

These are all segments for which the Europe Photonics market share is above its 15% average share (Figure 2). The total European Photonics production in these segments amounts to close to €60 billion, which is more than 45% of the total European Photonics production in 2022 (€124.6 billion). If European industry fails to produce the Photonics products and technologies considered in this white paper, it would require large imports from non-European manufacturers and produce supply chain risks for the six important segments of the European Photonics industry listed above.

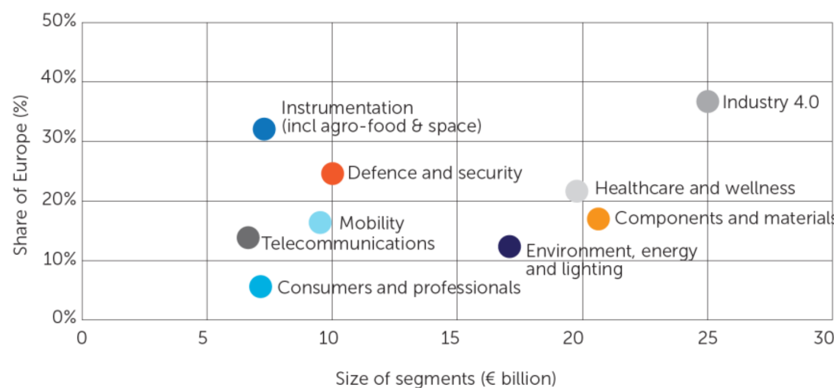


Figure 2: European photonics industry – % market share and value by segment (The average market share of European Photonics is 15%). Source: Tematys/Photonics21, 2023.

Securing Europe's supply of imagers and PICs requires advanced R&D work, but this is not enough. Investments in manufacturing capabilities are also needed. As pointed out in the Commission Staff Working Document for A Chips Act for Europe[4] (Figure 3), Europe is lagging in investments compared to the other geographic areas.

[4] https://ec.europa.eu/newsroom/dae/redirection/document/86690

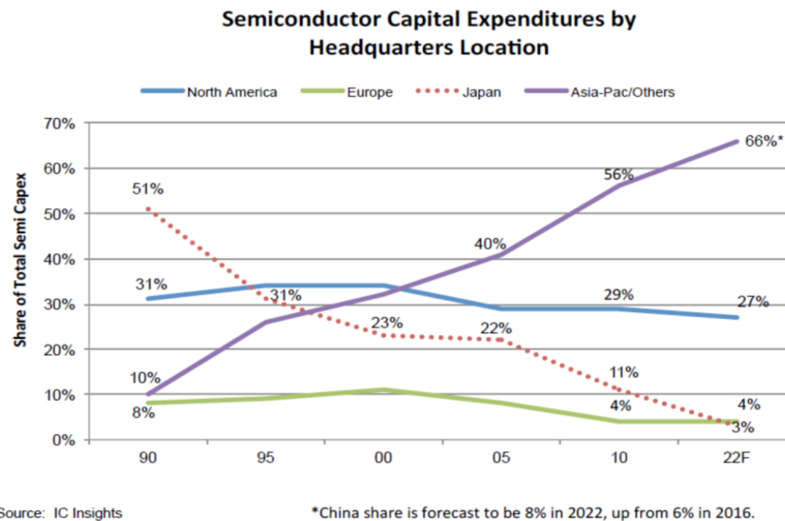


Figure 3: Evolution of capital expenditure in the semiconductor sector by region (based on headquarters location – Source IC insights 2022)

Europe’s share in capital expenditures (CAPEX) is at 4% since 2010. This is key to understanding why Europe’s semiconductor market share in manufacturing capacity is only at 7.2% and in value at around 10%.

This is confirmed by the EAC International Consulting report “Political Steering Processes in China in Core Segments of the Photonics Industry”[5]. Daniela Bartscher-Herold, Partner at EAC Munich and co-author of the EAC study said, “Our latest market research reveals that China’s strategic investments leveraged through its regional cluster funds alongside its national funds specifically for integrated photonics have helped the region advance as a critical technology leader.”[6]

Considering the time required for building semiconductor fabrication plants and the time for the process optimisation of the first industrial deployment (FID), it needs to be anticipated by four to five years compared to the volume manufacturing start date. The risks associated with this type of investment make it difficult to finance. Private investment requires public support in the form of the First-of-a-Kind mechanism to achieve the EU’s ambition to reach 20% of global market share by value.

5. Impact on European Citizens

The lack of support by Europe for the photonics technologies/products identified as ready to transition to 300 mm would be:

- The inability of Europe to offer competitive products
- The loss of market shares and jobs in these technologies/products sectors.

The academic sector adapts the curriculums it offers to the job market to maximise students’ employment after graduation. With less demand for photonics skills, the education provided in the photonics sector would be reduced. Without a well-educated workforce in the Photonics field, it becomes even more difficult to start new businesses and support existing ones. Losing ground in a technology starts a vicious circle that is difficult to break. This is certainly a problem for businesses. It is also for European citizens who will have difficulties having photonics education opportunities in Europe and joining a high CAGR sector that turns out to be scientifically and technically very exciting.

[5] EAC_VDI_TZ_Political_Steering_Processes_in_China_Final_Report_C3.pdf (photonics21.org)

[6] https://www.photonics21.org/download/news/2024/P24_04_-_EAC_REPORT_-_China_Political_Steering_Version_final_website.pdf

The weakness of the imagers and PICs sectors in Europe would put Europe at a higher risk of a shortage of supplies of these products. The semiconductor shortage was dearly experienced by the European auto sector, which lost an estimated 100 billion Euros in 2021-2022 [1]. The UK parliament report on the Supply of Semiconductor Chips [7] made the impact analysis broader and listed the associated documented impact for citizens:

- delays, shortages, and higher prices for consumer technologies
- economic losses for businesses leading to job volatility
- national security issues (semiconductor chips are integral to defence technologies)
- potential disruptions to critical national infrastructure (for example, power grids, communication and transportation networks and financial systems all rely on semiconductor chips)

Concerning specifically the space and defence sectors, as pointed out in the Commission Staff Working Document for A Chips Act for Europe[4], "The strategic importance of these two sectors is significant for Europe, thus creating the urgency of reducing the dependence of the EU industry from non-EU semiconductor suppliers. The inability of the EU space and defence industry to autonomous and unrestricted access to semiconductors could have a considerable impact on the competitiveness of the sector, the security of EU citizens and the EU's strategic autonomy."

Finally, as explained in §4, the European sectors using imagers and PICs for their products would require large imports from non-European manufacturers. With this comes the additional risk of Hardware Trojans in the imported semiconductor chips. Some Trojans will seek to change the functionality of the chip; others will choose to degrade performance or completely deny service offered by the chip; some will prefer only to leak information. Hardware Trojans can be added at different stages of the semiconductor chip supply chain. The attacker's capability or threat level decreases as the chip progresses from design to synthesis & verification, fabrication, testing and distribution[8]. The security risk of chips for which the first phases are not done in Europe would thus be higher, requiring the implementation of advanced detection methods from the importer. For European citizens, there would still be a higher probability of significant impacts, for example:

- confidentiality breach and critical infrastructure malfunction or disruptions using imported telecommunication PICs
- safety/security issues in mobility and surveillance with using imported thermal imagers

[7] POST-PN-0721.pdf (parliament.uk)

[8] https://ietresearch.onlinelibrary.wiley.com/doi/epdf/10.1049/iet-cdt.2020.0041

6. ANNEX A1 – Infrared Thermal Imagers

6.1. Overview

Uncooled LWIR (Long Wave Infra-Red) imaging is based on microbolometer FPA (Focal Plane Array) optimised for the spectral range of 8-14 µm. Each individual microbolometer absorbs the incoming electromagnetic radiation, and its temperature rises proportionally to the LWIR photon flux.

A microbolometer is a suspended membrane that absorbs the optical flux. The membrane supports a thermometer made of a thermoresistive material that measures its temperature increase. The microbolometer must operate in a vacuum to limit heat convection. Its membrane is floating and connected to the readout circuit (ROIC) via narrow arms to limit heat conduction while providing an electrical connection. A microbolometer is a micro-electromechanical system (MEMS).

The temperature increase of the bolometer is very small, and the measure requires complex circuitry to balance the FPA temperature variations and the self-heating of the thermometer and compensate for technological dispersions. The ROIC acquires, amplifies and multiplexes the electronic signals resulting from each pixel's microbolometer response to the temperature. It controls the image acquisition sequence (integration time and the imag e acquisition time as well as other settings) and delivers a raw video signal. The image is acquired line by line in a rolling shutter mode. The ROIC output digital signal frequency must be compatible with the system's needs in terms of frame rate.

Microbolometer imaging sensors are organised in a square grid pattern (FPA). The distance between the centres of adjacent microbolometers is called pixel pitch, which directly affects the FPA size and cost.

The ROIC is manufactured in semiconductor CMOS foundries, offering production to third parties who design semiconductors for their own purposes. The microbolometers are fabricated above the ROIC in MEMS foundries or fabs. It is a MEMS-above-IC production.

The mainstream sizes of IR sensors used for thermal imaging applications are from QVGA (320 x 240 pixels) format to SXGA format (1280 x 1024 pixels) or even full-HD (1920x1200) and pixel pitch distance between 17 µm and 8 µm. The Noise Equivalent Thermal Difference (NETD) measures the pixel thermal sensitivity and is typically in the range of 40-50 mK. The readout circuit is designed on a mature node (>90 nm) and fabricated on 200 mm wafers. The supply chain is fully 200 mm.

To further enhance the performance and miniaturisation of uncooled LWIR imaging systems, the integration of advanced optics modules, including meta-optics, is crucial. Metaoptics, which leverages advanced nano-micro-structured photonics to manipulate light at sub-wavelength scales, offers significant advantages in reducing the size and weight of optical components while maintaining or even improving their performance. Moreover, meta-optics can be engineered to exhibit specific optical properties, such as improved transmission efficiency and reduced chromatic aberrations, which are essential for high-quality imaging. These innovative ultra-thin and flat optical elements, in combination with refractive/diffractive freeform optics, can replace traditional bulky lenses and filters, enabling more compact and lightweight imaging systems. Integrating meta-optics with microbolometer FPAs could lead to significant advancements in the development of next-generation miniaturised imagers, opening new possibilities for portable and wearable thermal imaging applications.

6.2. Applications

Infrared thermal imagers are used mainly for four types of applications. These applications, listed by decreasing number of imagers shipped in 2022, are industrial, defence & aerospace, consumer and automotive. In 2022, the total

number of thermal imagers shipped was about 2.4 million units. For automotive alone, it was only about 200,000 units, mainly used for luxury cars[9].

Automotive

On 29 April 2024, the US National Highway Traffic Safety Administration (NHTSA) finalised a new Federal Motor Vehicle Safety Standard that will make automatic emergency braking (AEB), including pedestrian AEB, standard on all passenger cars and light trucks by September 2029. This safety standard is expected to reduce rear-end and pedestrian crashes significantly.

NHTSA projects that this new standard, FMVSS No. 127, will save at least 360 lives a year and prevent at least 24,000 injuries annually. AEB systems use sensors to detect when a vehicle is close to crashing into a car or pedestrian in front and automatically apply the brakes if the driver has not. Pedestrian AEB technology will detect a pedestrian in both daylight and darker conditions at night. This will significantly reduce injury or property damage and associated costs from these crashes.

The new standard requires all cars to be able to stop and avoid contact with a vehicle in front of them up to 62 miles per hour (100 km per hour) and that the systems must detect pedestrians in both daylight and darkness. In addition, the standard requires that the system apply the brakes automatically up to 90 mph (145 km per hour) when a collision with a lead vehicle is imminent and up to 45 mph (72 km per hour) when a pedestrian is detected.[10]

Vehicle OEMs have already, for some years, voluntarily offered AEB systems operating based on forward-looking visible light cameras and radar. While these systems perform admirably in the daytime and at lower speeds, today's systems are far less effective at night, particularly with respect to pedestrian AEB[11]. FMVSS 127 mandates AEB systems for future new US light vehicles and sets minimum performance standards, which include pedestrian crash avoidance in darkness at higher speeds than current systems can achieve. Thermal sensing can expediently and cost-effectively help OEMs augment AEB system performance to meet the new US regulations.

The European Union approved in 2020 a Road Safety Policy Framework 2021-30[12], with the aim to halve the number of fatalities and serious injuries on European roads by 2030. This aim is a milestone on the path to achieving Vision Zero by 2050.

Today, Europe relies essentially on EuroNCAP tests to evaluate the active and passive security of new vehicles. The fatality rate of vulnerable road users (VRUs) in difficult visibility conditions is very high: 70% of VRU fatalities happen in bad visibility conditions. To address this problem, NCAP organisms are starting to introduce test scenarios in degraded visibility conditions. In the Euro NCAP 2023 standard, two night-time scenarios were added: one with urban lighting and one with a low beam or high beam in the absence of urban lighting. VRUs in these scenarios are adults, children, bicyclists and motorised two-wheelers. More stringent night-time tests (low beam, no urban lighting, and glare from another vehicle) are added very progressively because of the poor efficiency of existing systems in degraded visibility conditions.

The Joint Research Centre (JRC), which is an independent, evidence-based knowledge and science centre supporting EU policies to impact society positively, showed[13] that in night-time scenarios, thermal cameras (especially

[9] Thermal Imaging and Sensing 2022, Yole Intelligence, 2022. (Report updated in 2024, see Ref. 17)

[10] https://www.nhtsa.gov/press-releases/nhtsa-fmvss-127-automatic-emergency-braking-reduce-crashes

[11] https://newsroom.aaa.com/2019/10/aaa-warns-pedestrian-detection-systems-dont-work-when-needed-most/

https://www.iihs.org/news/detail/pedestrian-crash-avoidance-systems-cut-crashes--but-not-in-the-dark

[12] https://www.europarl.europa.eu/doceo/document/A-9-2021-0211_EN.html

[13] https://todaynecessity.com/downloads/tinnes-sebastien-absr23.pdf

high-resolution ones) proved very effective up to 150m detection and that low-Resolution Thermal cameras can prevent pedestrian collisions in urban conditions.

Industrial, Defence & Aerospace, and consumer Thermal Imaging

Within the industrial, defence & aerospace, and consumer thermal imaging segments, two types of thermal imaging are in use: simple vision, which only requires getting a contrast in the image and thermography, which makes a radiometric measurement at each pixel of the image to evaluate the temperature of the objects in the image. Only the industrial segment uses thermography. The use cases in these three segments include:

- Industrial:
    - Thermography for building inspection (water leaks, electric boards)
    - Thermography for process control
    - Thermography for elevated body temperature measurement
    - Vision for Surveillance CCTV
    - Vision for firefighting
    - Maritime surveillance
- Defence & Aerospace
    - Military-enhanced vision and weapon sights
- Consumer
    - Ruggedised smartphones

6.3. Market Characterisation

Automotive

To be able to adopt the thermal imaging solution for the car environment sensing of AEB systems, automotive tier ones need a camera that can satisfy NHTSA requirements with a camera under €100. This price includes the thermal imaging sensor, the pre-processing, the optics, the integrated electronics and the packaging.

This objective is compatible with the existing technologies[14]. The first generation of thermal AEB cameras will use 12 µm pitch sensors.

The following generations of thermal AEB cameras will need to improve in performance while decreasing their price. Performance improvement will require higher-resolution sensors to detect and identify pedestrians at longer ranges. This can be achieved with increasing the image format, i.e. the number of pixels. For the thermal imager sensor surface and cost to stay steady or decrease, the pixel pitch will have to decrease. The pixel pitch of the second generation of thermal imaging sensors for AEB will thus be in the 8 µm range, and it will continue to go down with the following generations.

In parallel to pixel pitch reduction, there will also be a demand for easier integration and image signal processing. Today, an image signal processor (ISP) chip is necessary next to the thermal imager to perform basic operations like non-uniformity correction (NUC) and shutterless operation. The integration of the ISP functions directly in the thermal imager will be a clear competitive advantage. Already today, R&D thermal imagers in the development phase have started to offer some ISP functionalities[15]. This will become the norm. Moreover, for compactness and power consumption limitation, more advanced image processing and artificial intelligence (AI) processing is best done "at the

[14] https://todaynecessity.com/downloads/bendix_de_meulemeester_asbr23.pdf

[15] "Monocular thermal imaging for pedestrian detection and ranging", Eugene Petilli, SPIE, Optical Engineering, March 2023, Vol62(3)

edge" as close as possible to the sensor. For this purpose, 3D wafer stacking is the best solution. This is the approach used by Sony for their Intelligent Vision Sensor, which integrates artificial intelligence (AI) at the edge using 3D stacking[16]. Such a sensor enables high-speed edge AI processing within the sensor unit and reduces power consumption and communication costs. Moreover, each end-user can configure the intelligent imager for its own application by software and specific deep learning, making it adaptable to a large range of applications (automotive, smart cities, industry 4.0 ...). Sony's Intelligent Vision Sensor operates in the visible light wavelength range, but the concept can also be adapted to other types of imagers, in particular AEB thermal sensors, which require AI identification of pedestrians and obstacles.

Finally, the finalisation this year of the NHTSA's new regulation making pedestrian AEB mandatory in new vehicles starting September 2029 will make the demand for thermal imagers manufacturing increase rapidly. The anticipated adoption rate of thermal AEB systems in new vehicles and market volumes are shown in Figure 5.

Industrial, Defence & Aerospace, and consumer Thermal Imaging

For the already established thermal imaging segments like industrial, and defence & aerospace, high performance is the priority. The trend is towards:

- Smaller pixels
- Larger formats
- Additional functionalities
- Higher frame rates
- Higher sensitivity
- Multispectral capability for emissivity extraction and absolute temperature measurement
- Multispectral capability for gas identification
- Global shutter image acquisition mode to avoid image deformations of fast-moving objects (jelly effect). Visible light imagers with such acquisition mode have been available in high volume production since 2018 at ST and started to be manufactured for the automotive market in 2022 (Figure 4).

[16] Sony to Release World's First Intelligent Vision Sensors with AI Processing Functionality: https://www.sony.com/

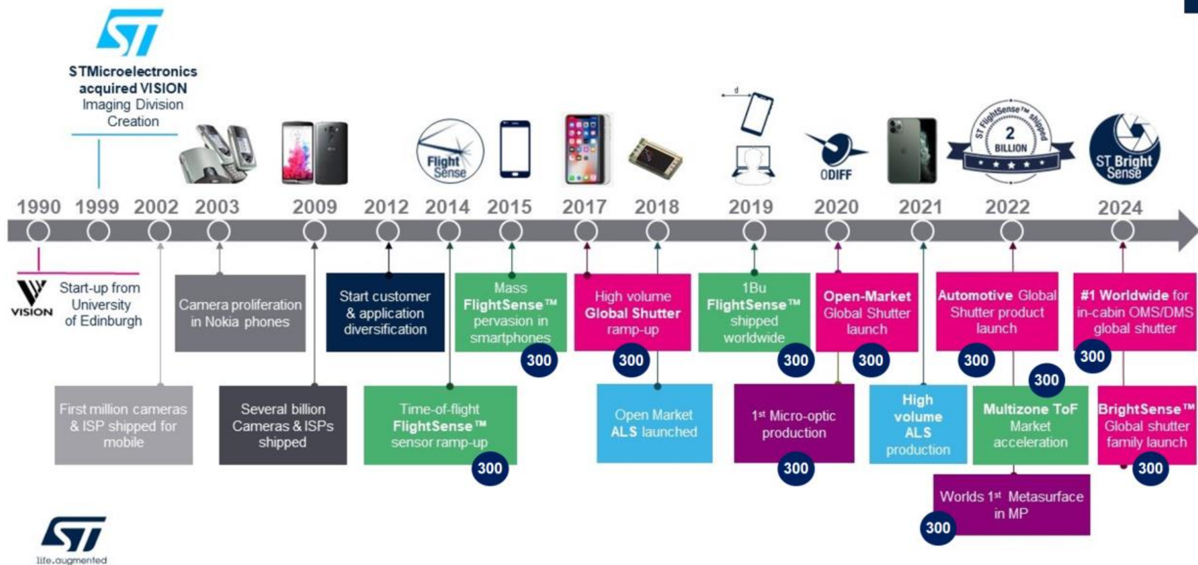


Figure 4: ST visible imaging technology (source: ST presentation at Photonics21 online seminar on Photonics on 300 mm)

6.4. MOTIVATIONS FOR 300 MM

At the turn of the century, ROICs were built from wafers with diameters of 150 mm for QVGA format sensors with 45 µm pixel pitch. Between 2010 and 2020, a new generation of MEMS on 200 mm CMOS wafers emerged. It became the latest mainstream for thermal imagers with 17 to 8.5 µm pixel pitch and VGA to Full HD formats.

The automotive market needs identified in §3 will require the advanced capabilities of 300 mm technologies:

- Sub 90 nm nodes for digital IC: sub 90 nm nodes are mandatory for adding functionalities to thermal imagers at the currently commercialised most advanced pixel pitch (12 µm) and furthermore still being able to offer these functionalities and high-speed serial links in products with smaller pixel pitch (<12 µm).
- 3D stacking technologies for edge image processing: the most advanced 3D packaging technologies are available on 300 mm wafers. They will be necessary to perform hybrid bonding between micro-bolometer thermal imager wafers and artificial intelligence (AI) chips on more advanced nodes 300 mm wafers.
- Advanced packaging solution for wafer-level optics integration
- High yields: Advanced photolithography process are required for advanced nodes CMOS process but also for achieving high yields during the MEMS above IC part of the process of small pitch devices (<12 µm). Indeed, the features to be defined for small pitches cannot be defined reliably with 200 mm photolithography tools.
- Decreased wafer processing cost per unit surface
- High Capacity

200 mm wafer technologies might also become obsolete in the 10 to 15 years to come. The transition of LWIR imaging technology to 300 mm ROIC appears inevitable. IR-FPA supplier leaders will design and fabricate their ROIC on 300 mm CMOS technology (<90 nm). Micro-bolometer technologies must adapt to the new ROIC formats.

For high-performance markets, 300 mm capabilities, sub-90 nm nodes and advanced integration technologies are key to developing sensors that satisfy market requirements.

6.5. Market trends

Automotive

Imaging for automotive is a fast-growing market. In the coming years, Original Equipment Manufacturers (OEMs) are expected to integrate an increasing number of thermal imaging technologies in vehicles. The basic trend is explained by two main factors: increasing demand for car automation supported by cost-effective technologies combined with upcoming stringent safety regulations:

- On the one hand, the level of autonomy of cars is increasing, and it relies strongly on more affordable imaging technologies.
  As of today, thermal imagers are mainly used for night vision in vehicles. Thermal cameras will also be used for another use case in the near future, as described earlier in the paper: autonomous emergency braking (AEB).
  Thermal imaging will most certainly find traction through those two applications, night vision and AEB, driving demand for significant volumes if, and only if, the technology comes with continuous cost reduction. Indeed, to compete with affordable visible cameras, cost is a major challenge for thermal imagers.
  The thermal imaging technologies' increasing performance and decreasing prices, especially at the micro-bolometer level, encourage market expansion in volumes and support wider adoption by the market.
- On the other hand, the automotive industry is subject to an increased focus on safety coupled with more rigorous regulations.
  The emergence of new regulations in the US on AEB systems will be enforced by September 2029. Mass adoption of thermal imaging technologies in the US will most certainly be a direct consequence. Similar regulations are expected in the coming years in both European and Asian markets.
  More globally, strict safety level requirements will soon be imposed on tier-one companies and OEMs in the automotive sector to meet the newly adopted regulations.

Furthermore, the automotive thermal imaging market volume numbers are being estimated by using the following assumptions:

- Night AEB is the only use case considered to collect data;
- Following the NHTSA regulation, we consider that OEMs will equip all new vehicles sold in the US starting in 2029. Shipment of the corresponding thermal imagers has to be anticipated for at least one year;
- Asia will implement the same regulations quite fast when a two-year gap is to be anticipated in Europe;
- Luxury vehicles will be equipped first, even before the enforcement of NHTSA regulations;
- Thermal imagers used for night AEB are competing with other technologies such as LIDAR, high-resolution CMOS, Matrix LED highlights, etc.

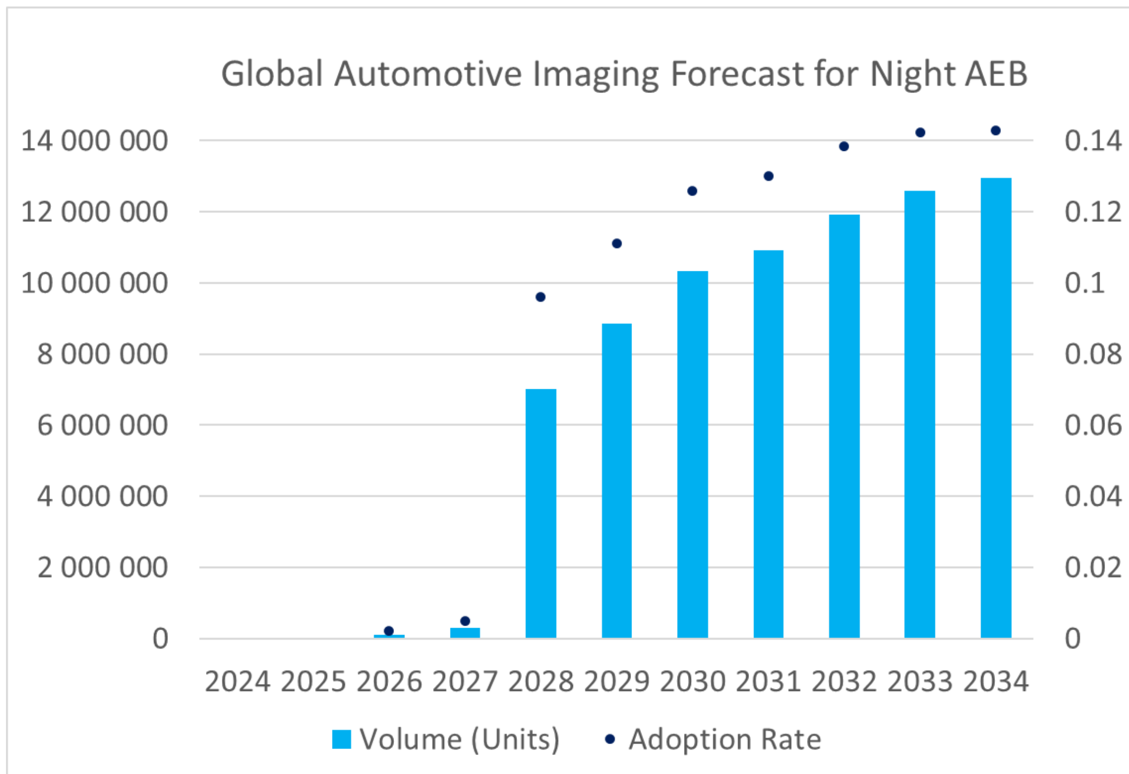


Figure 5: Anticipated adoption rate of thermal AEB systems in new vehicles and market volume (based on LYNRED analysis).

The automotive thermal imaging industry is expected to grow by a factor of about 50 in less than ten years, from around 200,000 pieces in 2022 to more than 10 million units per year starting in 2030. The adoption rate of thermal imaging technologies is projected to be sharply exponential during the two years preceding the implementation of the regulations and is expected to rise above 10% before 2030. This is the trend observed for previous safety technology adoption by the automotive sector, like airbags, lane departure monitoring, and blind spot monitoring.

To conclude, even though cost reduction remains a challenge, AEB is an upcoming promising application for thermal imaging to generate volumes. Automotive thermal imaging is expected to shift from a niche market to a large-volume market quickly.

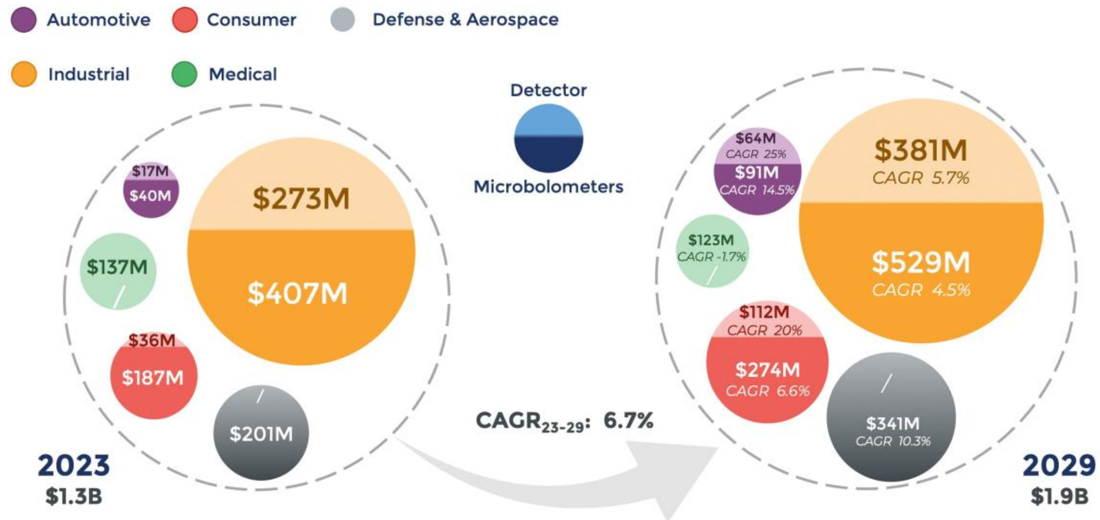
Industrial, Defence & Aerospace, and consumer Thermal Imaging

Yole Group's Thermal Imaging and Sensing 2024 market study [17] anticipates the market evolutions of the other applications of thermal imaging: industrial, defence & aerospace, and consumer to be at CAGR of respectively 4.5%, 10.3% and 6.6% (Figure 6). Compared to the automotive market, these are closer to "established" market evolutions. The strongest evolution among these three markets is in the defence & aerospace segment. It is linked to the present geopolitical instabilities and conflicts.

[17] Thermal Imaging and Sensing 2024, Yole Intelligence, April 2024

2023-2029 THERMAL DETECTOR AND MICROBOLOMETER DEVICES MARKET BY END-MARKET

Source: Thermal Imaging and Sensing report, Yole Intelligence, 2024



www.yolegroup.com | ©Yole Intelligence 2024

Figure 6: Expected market evolution for thermal detectors (limited to about 80x60 pixel arrays) and micro-bolometer imagers. Source: Thermal Imaging and Sensing 2024, Yole Intelligence, April 2024 [17].
Note that Yole Group issued this report before the approbation of the US regulation imposing pedestrian AEB in 2029. Therefore, the automotive market prevision depicted here does not fully account for the surge in thermal imagers it will create. Micro-bolometer devices' market value for automotive in 2029 is expected to be more than four times the Yole Group estimate. For a more in-depth analysis of the automotive market evolution, see §6.5 and Figure 5.

6.6. Sales and Jobs Forecasts

As described above, the US regulation imposing pedestrian AEB in 2029 will completely disrupt the CAGR forecast of the automotive thermal imaging segment, which was expected to be 12,1% for the 2022-2028 period [18]. Instead, the anticipated volume of thermal imagers for the automotive segment is poised to grow by a factor of 50 in the next decade. In 2029, about 8.8 million units will be needed. By 2033, more than 12 million units per year will be necessary to equip new vehicles with night AEB systems, as described above. The overall market value for micro-bolometer thermal imagers is thus expected to be worth € 1.6 billion in 2029.

All things being equal, a high demand for skilled workers will appear, more specifically dedicated to the production and delivery of the corresponding imaging components. Considering all micro-bolometer thermal imaging market segments, automotive, consumer, industrial, medical and defence & aerospace, we expect about 6,500 direct jobs to be involved in the thermal imaging market by 2029. For Europe, this is about 1,300 direct jobs with a market share of 20%, as ambitioned by the Chips Act. These convert to a total of more than 2,600 jobs in Europe when counting as well indirect and induced jobs [19].

[18] Imaging for Automotive 2023, Yole Intelligence, 2023.

[19] *Cf. Evaluation du Programme Nano 2017 – Rapport d'évaluation – https://www.gouvernement.fr/sites/default/files/contenu/piece-jointe/2021/06/nano_2017_rap_vf_2021-06-23.pdf*

7. ANNEX A2 – Photonic Integrated Circuits (PICs)

7.1. PICs Overview

PIC products and technology overview

Integrated photonics or photonics integrated circuits (PICs) involve the creation of complex optical functions through photonic circuits on a chip, enabling the generation, processing, and detection of confined light. PICs find applications across diverse industries, including digital connectivity, computing, agri-food, natural resources, security, transportation, industrial automation, aerospace, consumer electronics, and healthcare. A recent whitepaper[20] by the European Association for Smart Systems Integration (EPoSS) discusses the application of integrated photonics and its relevance for European industries. It emphasises the importance of achieving strategic sovereignty and developing a secure digital society with a focus on sustainability (Green Deal).

Today, integrated photonics plays a crucial role in the datacom and telecom industry, and there is a growing interest in incorporating integrated photonics into solutions for the AI-powered digital and connected world. It marks the start of a significant growth phase for integrated photonics, with applications extending beyond telecom into sectors such as mobility, healthcare, agri-food, and quantum technology. Analysts are optimistic about the double-digit growth projected for the photonic IC industry.

Europe has historically led in the research and innovation of integrated photonics. However, the region now faces a critical juncture where it needs to elevate its technological readiness to remain competitive globally. Europe's ability to leverage the full economic benefits of integrated photonics will depend on its capability to scale production and compete with global players in key technology areas such as 300-mm integrated photonics.

Silicon photonics emerged as a highly sought-after technology, offering a versatile platform that can incorporate advanced materials. The rising demand for high-speed, low-latency, and energy-efficient solutions in AI, data centres, and high-performance computing (HPC) highlights the importance of 300-mm silicon photonics. Commercially available silicon photonics-based solutions mainly rely on 300-mm technologies developed by world-leading foundries like Intel, TSMC, Samsung and GlobalFoundries. Market projections (Silicon Photonics 2023, Yole Intelligence[23]; see Figure 7) suggest continued growth in 300-mm silicon photonics. For Europe to stay competitive, it needs to enhance its commercial-grade 300-mm silicon photonics capabilities.

[20] https://www.smart-systems-integration.org/media/2246

Figure 7: 300-mm equivalent SOI wafers forecast (2021 – 2028). Source: Silicon Photonics 2023, Yole Intelligence, November 2023.

In addition, the variety of applications enabled by PIC continues to grow, highlighting the need for diverse PIC technology platforms to meet specific application requirements. The industry is actively integrating advanced packaging and heterogeneous integration to support a broad range of applications. Figure 8 illustrates the evolution of SOI-based silicon photonics into a versatile platform capable of incorporating various PIC technologies.

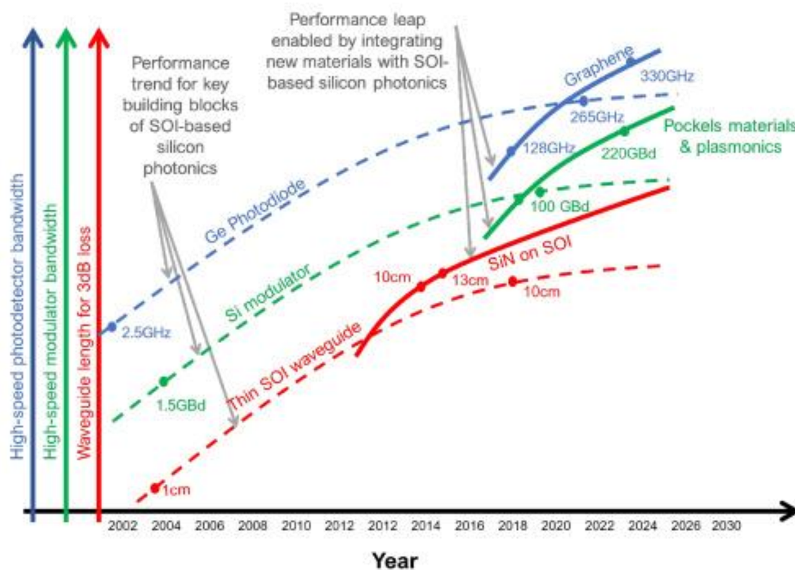


Figure 8: The graph illustrates the advancement in performance of key SOI-based silicon photonics building blocks. The thick, solid lines indicate improved performance achieved through the integration of new materials. In contrast, the thin solid lines represent the standard performance. The data is presented for telecom wavelengths, with the dots on the lines indicating early and

state-of-the-art results for each trend. Figure reproduced from Roel Baets and Abdul Rahim, "Heterogeneous integration in silicon photonics: opportunities and challenges: opinion," Opt. Mater. Express 13, 3439-3444 (2023)[21]

Despite Europe's expertise in photonics research, the region lacks the industrial capacity to produce high-TRL 300-mm silicon photonics at scale. The European Commission has been actively supporting the development of integrated photonics, including infrastructures, through various funding programs, including Horizon Europe Calls, the Quantum Flagship, IPCEI initiatives, and many more. The launch of the >€40 million photonixFAB project in 2024, co-funded by the EU and its members, marks a significant step towards establishing a 200-mm integrated photonics industrial supply chain in Europe. However, Europe's strategic vision must extend further. The upcoming Chips JU's Photonics Pilot Line, although many processes are not yet fully aligned for 300-mm production, emphasises the importance of progressing to full-300-mm integrated photonics. Building industrial capacity for PIC manufacturing on 300-mm technologies is the next necessary step for Europe to compete globally. Scaling up to 300-mm wafer production will enhance Europe's ability to produce high-performance PICs, ensure compatibility with electronic IC processes, support future innovations in photonic technologies, and secure its technological sovereignty.

The following section of the whitepaper delves into the European standpoint on PICs utilising 300-mm technology. This section articulates the necessity of investing in 300-mm technologies to bolster the competitiveness of the European PIC industry in the global market.

Today, the chip volume of Photonics IC (PIC) is relatively small compared to that of Electronic IC (EIC). The PIC volumes will continue to lag behind EIC volumes in the future as well. In the era of AI, it is becoming increasingly clear that EICs will seek PICs to meet the price and performance specifications.

PIC material platforms and wafer sizes

The primary material systems utilised for PICs encompass silicon-on-insulator (SOI), silicon nitride (SiN), and indium phosphide (InP). While several other semiconductor materials offer photonic functionalities, they are predominantly at the device level and fall outside the scope of this section. Figure 9(a) displays the mainstream and emerging material systems for PICs. Figure 9(b) lists existing and upcoming applications associated with these material systems. The main application of PICs today is in high-speed transceivers, which offer energy-efficient and low-latency optical connectivity for various distances. The diversity of materials used in PICs arises from the fact that no single platform can offer all the technical attributes required by a diverse range of applications. It is pertinent to mention that mainstream material systems like SiN provide more flexibility in integrating novel materials (such as ferroelectrics, 2D materials, and others) with the baseline SiN platform.

The field of integrated photonics is currently following four technological trends:

- 1. Wafer-scale heterogeneous integration of different PIC material systems to enhance performance
- 2. PIC manufacturing on larger diameter wafers to improve scalability and production efficiency
- 3. Enhanced integration between electronic ICs and photonic ICs for optimal functionality
- 4. Improvement in the functional performance of key photonic IC building blocks to meet the increasing demands of industry.

[21] https://doi.org/10.1364/OME.509531

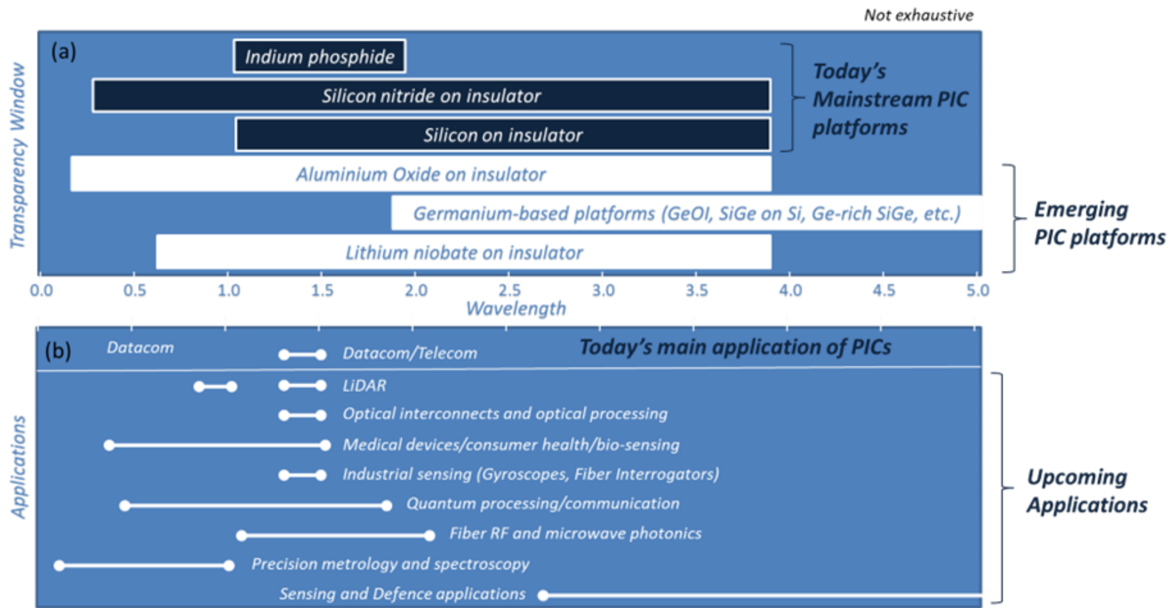


Figure 9: Mainstream and emerging photonic IC platforms and their transparency window that leads to the enablement of applications for various markets.

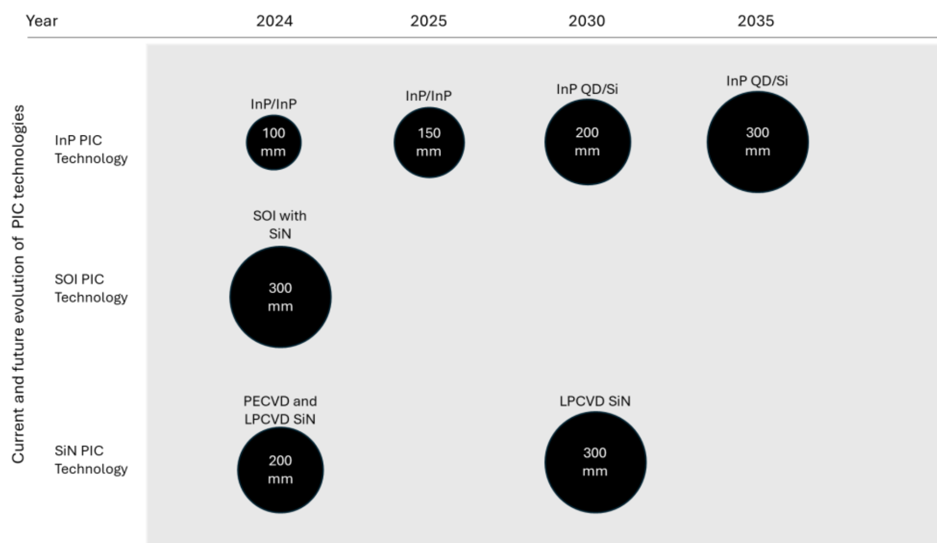


Figure 10: Comparison of the present and expected wafer sizes used by the three mainstream PIC technologies.

As of now, the predominant PIC technologies are InP, SOI, and SiN. Presently, there are limited commercial offerings of 300-mm SOI PICs available with a limited capacity in Europe. SiN PICs are currently produced on 200-mm wafers, but there is potential for future growth and a likely transition to 300-mm substrates. InP PICs are presently manufactured on 100-mm wafers, with plans announced for transitioning to 150-mm wafers. Layer transfer of InP on 300-mm Si substrate is on the roadmap.

Figure 10 provides an illustrative comparison of the wafer sizes used by the three mainstream PIC technologies currently and in the future. Foundries are producing SOI PICs using 200-mm and 300-mm technologies, with 200-mm foundries being more prevalent in the market. Asian and American pure-play 300-mm foundries offer PIC manufacturing services, while Europe needs to enhance its 300-mm capabilities. STMicroelectronics in Europe, Intel in the USA, and Samsung in South Korea have developed proprietary 300-mm SOI PIC technologies. European research labs IMEC and CEA-LETI have demonstrated significant advancements in 300-mm SOI PIC technology. AIM Photonics in the USA and AIST in Japan have further advanced 300-mm SOI PIC photonics. SiN PIC platforms are predominantly based on 200-mm or smaller wafers. However, some 200-mm and 300-mm SOI platforms also incorporate a SiN layer in their technology stack. Today, the demand for stand-alone SiN PICs does not mandate a

transition to 300-mm technologies. Ongoing commercial developments continue to focus on 200-mm SiN PICs, while several sub-200-mm technologies also exist. Recently, a medium-volume foundry initiative in the Netherlands has been announced, and the foundry named New Origin will offer a 200mm SiN platform with the possibility of novel material integration. Research institutions such as IMEC and LETI have made notable progress in developing 200-mm SiN PIC technologies. Similarly, institutes like IMB-CNM offer SiN PIC technologies on smaller wafers.

As elements in the next generation of photonic components, PICs require high performance, high compactness, and low cost. When speaking about highly integrated and low-cost semiconductor devices, naturally, silicon-based technologies look to be candidates of choice. However, even if some breakthroughs have been observed in recent years, silicon-based technologies remain very limited in generating photons. They are now a stand-alone solution for photonics. At the same time, III-V semiconductor materials, despite wafer size limitation typically 200mm for GaAs and 100mm for InP, remain the embattle solution for photon generation and emission.

Based on this statement and considering that both technologies have their limitation, such as poor photon emission for Si and limitation in wafer size and then cost for III-V, it seems obvious that the closed co-integration of III-V and silicon technologies is the only option to get at the same time, highly integrated and cost-effective PICs.

This co-integration of III-V material on 300mm Si wafers can be achieved by a direct regrowth of III-V material on Si, but this is limited to some very specific cases. It is more usually achieved in one of the several ways where the three main patches are described here:

- III-V material hetero-epitaxy on Si wafer (also called InPoSi)
- III-V epitaxial die bonding on Si wafer (also called die-to (wafer bonding) or Sipho)
- III-V chiplets integration on Si, SOI or SiN wafer via Micro Transfer Printing (MTP) or flip-chip

A similar co-integration approach has also been developed over the recent years for other functional materials, including electro-optic materials such as lithium niobate and barium titanate.

All these techniques have different advantages, maturity levels and specificities, which can be well adapted to some applications and not to others. Table 1 below provides a first benchmark of the benefits and drawbacks of the different technologies.

Table 1: Comparison of the maturity levels, advantages and drawbacks of the main co-integration technologies.

	Maturity level	Advantages	Drawbacks
III-V hetero-epitaxy	TRL3-4	• Compatible with regular 300mm Si wafer processing	• Epitaxy process still critical (structuration and 300mm capability) • The hot temperature epi process might not be compatible with patterned Si wafers
Die-to (wafer bonding)	TRL>7	• Compatible with regular 300mm Si wafer processing • Compatible with patterned Si wafers	• The wafer bonding process is still critical with challenges in a defect-free interface (different crystal structures and lattice constants), thermal mismatches between III-V materials and Si, scalability and yield...
Micro transfer printing (MTP)	TRL4-5	• III-V Chiplet processed on a regular III-V foundry front-end line • The high versatility of the process (multichip, multi-technologies, high throughput)	• Limited thermal management due to BCB insulating layer between III-V chiplet and Si wafer

			• Chiplet and Si wafer codesign for optical coupling management
Flip-Chip bonding	TRL>7	• III-V Chiplet processed on a regular III-V foundry front-end line • Improved thermal management vs MTP	• Limited throughput • Requires local back-end removal

This benchmark has to be refined depending on the targeted applications, which will be detailed in the next paragraph.

7.2. APPLICATIONS

An earlier published whitepaper on integrated photonics by Photonics21 illuminates the essential drivers of photonics IC technology and its correlation with the European Green Deal, strategic sovereignty, and the digitisation of society. The following section provides a concise summary of the key insights from the Photonics21 whitepaper on integrated photonics[22].

Optical communications have been essential for global digitalisation, offering high capacity, energy efficiency, and long reach. Integrated photonics has played a crucial role in meeting the increasing demand for higher data rates, lower costs, smaller footprints, and lower power consumption. To achieve higher data rates, more efficient optical materials need to be integrated with established platforms like silicon photonics. New packaging approaches and closer integration of functional blocks are necessary to accommodate higher bandwidths and denser operation of transceiver modules. Improved modulation formats and spatial parallelisation using several fibres or multicore fibres are becoming economically viable ways to improve optical link capacity. Further developments in integrated photonics are enabling communication devices with higher efficiency and lower power consumption to keep up with future demand in bandwidth.

High-Performance Computing (HPC) is vital for weather forecasts, molecular modelling, and AI advancements. HPC is probably the application where compliance of PIC technologies with the 300mm logic and memory technologies is highly desirable. Market analysts believe that optical connectivity for HPC will be the biggest driver for PIC technologies. HPC systems focus on PIC-based die-to-die interconnection technologies to efficiently move data among computing resources and improve overall bandwidth at all levels of communication. Developments for chiplet architectures and photonic interposers to improve bandwidth between chips are ongoing. Integrating different dies (chiplets) in the same package allows for cost reduction and optimum mix-and-match of technologies. Lowering overall interconnect power consumption also drives the industry towards packaging photonics close to electronic interconnects, known as "Optical co-packaging," achievable with PICs. In the long term, PICs will bring new computing paradigms, such as neuromorphic and analogue computing, and enable quantum computing through optical/photonic co-processors or photonic qubit realisation.

The modern world is facing environmental challenges such as climate change and pollution. We need reduced greenhouse gas emissions and air/water pollutants to address these risks. Photonic IC technologies offer cost-effective and efficient solutions for detecting and measuring dangerous substances.

The increasing global population and its impact on the environment call for greater efficiency and reduced environmental impact in the *agri-food* sector. Precision agriculture involves real-time measurement of growth parameters to control and optimise the production processes. Key trends include the development of more

[22] https://www.photonics21.org/download/ppp-services/photonics-downloads/White_Paper_on_Integrated_Photonics_-_EPoSS__Photonics21_-_ONLINEVERSION.pdf

autonomous processes, measurement of plant composition, and miniaturisation of sensing devices. Photonics offers real-time monitoring and control in agriculture and food processing, but high costs have limited its use. Integrated Photonics-based sensor systems have the potential to address these challenges by offering accurate, low-cost, and robust sensors for long-term use.

The industry is undergoing digitalisation and automation, replacing manual tasks with manufacturing robots, machine vision, and artificial intelligence. Integrated Photonics creates miniaturised sensors, imaging systems, and optical communication solutions for *industrial automation*. Integrated Photonics also offers autonomous driving systems in industrial settings, offering compact and efficient solutions for various manufacturing needs.

Integrated Photonics has numerous applications in healthcare. It can improve medical optical imaging, early disease detection, and enhance disease diagnostic tests. Integrated Photonics combined with energy-saving electronics is essential for developing wearables for long-term monitoring and non-invasive diagnostics. This technology also has potential applications in *consumer* electronics, such as smartwatches.

Photonic ICs will play a vital role in mobility, especially through LiDAR systems for autonomous driving and crash prevention in various vehicles. Additionally, photonic integrated circuits are making significant advancements in space applications, including laser communication terminals for inter-satellite communication and intra-satellite high-speed digital switching.

Integrated photonics is a key technology in advancing next-generation quantum technology systems for computing, secure communications, and sensors. Photonic IC can form the basis for quantum effects or facilitate other technical solutions by providing interconnectivity, readout, ion trapping, and external interface capabilities.

In the coming decade, the integrated photonics market is set to experience significant expansion, driven by key technological advancements and a surge in demand across various sectors. According to Yole Group's Silicon Photonics 2023 Report[23], considerable developments are anticipated in several areas, including Datacom, where optical communication and networking technologies are evolving rapidly. The market is also expected to benefit from global trends in telecommunications, such as xWDM (wavelength division multiplexing), which will enhance data transmission capabilities. Additionally, advancements in optical computing and sensing technologies are set to revolutionise applications in consumer electronics, healthcare, automotive, and beyond. Integrated photonics will be instrumental in meeting the growing need for high-speed data transmission and enabling innovative solutions across these industries.

7.3. Market Characterisation

For Datacom applications, photonic integrated circuits (PICs) are expected to achieve data transmission rates of up to 400 Gbps, driven by the increasing demand for faster and more efficient data transfer in data centres and network infrastructure. Ongoing research is targeting transmission speeds as high as 800 Gbps and beyond, which will be essential to support the exponential growth of data traffic, especially with the expansion of cloud services, artificial intelligence, and machine learning workloads. A key factor in boosting bandwidth is the integration of multiple wavelength channels using techniques such as Coarse Wavelength Division Multiplexing (CWDM) and Dense Wavelength Division Multiplexing (DWDM). These technologies enable PICs to provide approximately five times more bandwidth per fibre, achieving a throughput of 1 Tb/s, with future scalability up to 4 Tb/s as the number of wavelength channels and data rates per channel increase.

Power efficiency remains a critical consideration, especially in data centres where energy consumption is a growing concern. Current PICs aim to improve energy efficiency by a factor of five, reducing energy consumption to

[23] Silicon Photonics 2023, Yole Intelligence, November 2023

approximately 1 pJ per bit, with future improvements targeting even lower levels – down to 0.25 pJ per bit. Achieving these reductions in power consumption is crucial for the development of sustainable, energy-efficient data centres and high-performance computing systems that can meet the global demand for computing power without overwhelming energy resources.

Ultra-low latency is another key performance metric, particularly for applications that require real-time data processing, such as high-frequency trading, telecommunications, and autonomous systems. PICs are being designed to deliver latency of less than 10 ns with minimised jitter, ensuring the reliable and timely transmission of data in latency-sensitive environments.

In terms of reliability, PICs must be able to operate continuously for extended periods under demanding conditions. They are expected to demonstrate operational lifetimes exceeding 100,000 hours (over 11 years), which is critical for industrial applications that require long-term stability and minimal maintenance. Additionally, failure-in-time (FIT) rates must remain below 1 FIT, particularly for critical applications such as medical devices and aerospace systems, where even minor failures could have significant consequences.

Cost considerations are also important, especially as PICs transition from niche markets to high-volume manufacturing for Datacom applications. The target price for high-volume Datacom PICs is approximately €10 per chip, while custom or lower-volume products may range from €100 to €500, depending on complexity and specific requirements. However, the total cost of ownership (TCO) must also be taken into account. This includes not only the initial purchase price but also ongoing operational costs, such as energy consumption and maintenance. A focus on reducing TCO by up to 50%, particularly through energy savings, is critical for widespread adoption in energy-conscious markets like data centres.

On the manufacturing side, production capacity must scale to meet global demand. Production lines for PICs should be capable of fabricating over 10,000 wafers per year, with the flexibility to support small to medium-scale production for custom solutions. Scalability to 300-mm wafers is essential to leverage the cost advantages of high-volume semiconductor processes. This will help reduce the per-unit cost of PICs as demand increases.

Sovereignty and supply chain security are becoming increasingly important as geopolitical risks and global supply chain disruptions pose challenges to the semiconductor industry. Companies are prioritising the use of local and trusted supply chains, aiming to source more than 80% of critical components from within the European Union or allied nations. Compliance with regulations such as the European Union's REACH and RoHS directives is mandatory, ensuring that PICs meet stringent environmental and safety standards while also supporting sustainability goals.

In addition to Datacom applications, PICs are expected to play a crucial role in emerging quantum technologies, including quantum communication, computing, and sensing. To meet the demands of these markets, PICs must integrate seamlessly with quantum technologies such as quantum dots and entangled photon sources. Specific requirements include coherence times and entanglement fidelity greater than 99%, which are necessary for the reliable generation and manipulation of quantum states.

Finally, advanced packaging techniques are critical for addressing the challenges of miniaturisation and thermal management in high-density PIC systems. Techniques such as 2.5D integration and chiplet architectures enable the integration of multiple PICs and electronic components in a compact form factor while also improving thermal performance and scalability. These innovations will be essential for developing the next generation of high-performance, energy-efficient photonic systems.

7.4. Motivations for 300 mm

- Performance improvements brought by 300-mm technologies

    - Starting wafer (SOI) uniformity is considerably better for 300-mm than for 200-mm technologies. This substantially affects the wafer-scale uniformity of all devices and, in particular, wavelength-sensitive devices such as grating couplers, filters (MZIT, Ring), ring modulators, etc. Also, splitting ratios in couplers will be more uniform
    - Better critical dimension (CD) uniformity control over the reticule field and wafer impacts photonics waveguide losses and light group velocity inside the waveguides. Lower losses are observed on 300mm wafers compared to 200mm thanks to advanced photolithography (dry or immersion DUV) that reduces waveguides sidewall roughness)
    - 3D cross-section control of the photonic waveguides will benefit from the 300mm manufacturing equipment and manufacturing processes
    - 65nm process node 193-nm litho and 193-nm Immersion lithography would enable sub-wavelength structures and, hence, new functionality
- Cost improvements brought by 300-mm technologies
    - Reduced Wafer Handling Costs: Handling and processing larger wafers (e.g., 300 mm) can be more efficient in terms of equipment utilisation and labour costs compared to smaller wafers (e.g., 200 mm), potentially reducing overall production costs.
    - Possible cost reduction could be through better yields for using 300-mm tools (Note: 300-mm tools with 200-mm configuration would provide the same benefit for 200-mm wafer size)

Value-proposition of photonics on 300-mm technology

Firstly, larger-diameter substrates naturally facilitate a higher throughput of chips per wafer. Transitioning from a 200-mm wafer to a 300-mm wafer offers improved within-wafer and wafer-to-wafer thickness dispersion of the guiding photonic layer. For instance, in the case of SOI wafers, suppliers can ensure angstrom-level hill-to-valley surface roughness for 300-mm wafers and a two-fold enhancement in the thickness dispersion compared to 200-mm wafers. This precise control over the quality of the guiding silicon layer holds the promise of predictable and enhanced passive optical performance at the wafer scale, resulting in increased front-end yields and minimising the risks associated with scaling up volume production. The improved passive performance also provides a buffer against potential performance degradation from the BEOL processes.

Secondly, 300-mm technology enhances the process control of manufacturing for PICs thanks to access to an extensive array of advanced CMOS processing tools. A key advantage of using a 300 mm CMOS facility to develop a Si photonic technology is the availability of a large panel of processing tools featuring a large spectrum of possibilities. This advanced technology provides access to state-of-the-art lithographic tools, enabling smaller feature sizes with improved precision. Additionally, it allows for superior oxide-filling materials, paving the way for large-scale manufacturing of a new range of devices like subwavelength waveguide devices and inverse-design devices. The superior patterning quality offered by 300-mm technology results in enhanced performance of waveguides and waveguide devices. Addressing roughness on patterned photonic devices becomes vital, as it is a significant source of optical losses. With the scale of integration in photonic ICs increasing and the analysts forecasting that 75% of PICs' sales revenue will come from those with large-scale integration in the next three to five years, the demand for superior process control enabled by 300mm technologies at the lithographic and patterning levels intensifies.

Thirdly, in the field of photonic IC, a significant amount of innovation is currently concentrated at the device level. Access to a superior process toolset for 300-mm PIC technology provides a competitive advantage. This advanced toolset not only enhances the performance of existing device concepts but also facilitates the creation of new and innovative devices. For example, by leveraging the high alignment accuracy of reticle stitching with advanced 193-nm lithography, it is possible to develop a wafer-level optical interconnect to connect several processor and memory units on a 300-mm substrate.

The fourth aspect focuses on integrating advanced materials with PIC technologies, an area of intense interest because no single material can fulfil all the required functionalities or performance attributes. For example, SOI-based PICs lack lasing and optical gain functions, necessitating the integration of compound semiconductors like InP for light generation and optical gain. Techniques such as die-to-wafer bonding, flip-chip bonding, and micro-transfer printing exist at different stages of technical readiness. These techniques involve populating a 300-mm target wafer with small pieces of a source substrate, presenting complexities and potential yield implications. Ultimately, it becomes expensive and demands a complex supply chain. A more attractive route for heterogeneous integration is a layer transfer of advanced material onto the host 300-mm wafer, allowing easier handling of the subsequent process steps without impacting yield and cost.

Lastly, as mentioned earlier, the 3D integration of EIC/PIC is rapidly gaining significance. Over time, the convergence of EIC and PIC has evolved from utilising pluggable components to on-board optics and co-packaged optics. This seamless integration is now imperative for data centres and the high-performance computing (HPC) industry to achieve optimal efficiency and cost-effectiveness in optical connectivity. This progression toward tighter integration between photonic and electronic components will persist and extend to diverse applications. The actual development of PIC chiplets could utilise technologies from wafers of a diameter smaller than 300 mm. However, in most cases, it would be essential for a co-packaged structure to demonstrate flexibility and conformance with the infrastructure, processes, and toolsets of the host ASIC developed on a 300-mm platform. It encompasses ensuring compatible feature sizes on photonic chips and aligning with through-silicon vias (TSVs) to facilitate the integration of photonic technologies with 3D electronics technologies. Undertaking this co-integration is streamlined when conducted at 300 mm, given that tool developers have optimised their tools for this specific scale.

In conclusion, Europe must transition to 300-mm integrated photonics technology to maintain its leadership in the global photonics industry. Europe has a strong legacy in photonics research, and adopting 300-mm wafer technology will be crucial for scaling up production, enhancing competitiveness, and meeting the increasing global demand for advanced photonic integrated circuits. The shift to 300-mm technology offers several significant advantages: it enhances production efficiency by allowing more PICs to be produced per wafer, improves compatibility EICs, and supports the development of more complex and high-performance PICs. Major global companies such as Intel, TSMC, and Samsung have already integrated 300-mm technology into their processes, underscoring its importance. Currently, Europe is lagging in scaling up to 300-mm technologies, which are essential for producing advanced PICs in large volumes. This technology enables higher production rates, better process control, and the use of advanced materials, all of which are critical for advancing applications in AI, data centres, high-performance computing, as well as in sensing and quantum technologies. To remain competitive, Europe must accelerate its efforts to build 300-mm manufacturing capabilities. Investing in this technology will help Europe meet current demands and position itself as a leader in emerging areas such as co-packaged optics and large-scale photonic integration. Therefore, timely investment in 300-mm integrated photonics is essential for Europe to keep pace with global leaders and secure a strong position in the industry.

7.5. Market trends

In the coming years, the field of integrated photonics will see an evolution along the following dimensions.

Increased intimacy with electronics: The significance of photonic integrated circuits (PICs) is indisputable for driving optical connectivity. Figure 11 illustrates the revolution of EIC-PIC integration. Short-reach optical connectivity options come in the form of pluggable transceivers or co-packaged optics. Regardless of the specific approach, a more intimate integration of electronic integrated circuits (EICs) and PICs is critical for extracting optimal performance in optical connectivity. In the era of AI, optical connectivity stands as a promising avenue for offering high-speed, cost-effective, low-latency, and low-power solutions to connect GPUs and memories for high-performance computing applications. Tighter electronic-photonic integration is necessary for optical connectivity at all ranges. The future product

architecture of PIC-enabled applications for other markets will also necessitate the same. Market analysts have projected a substantial shipment of 22 million ports for optical connectivity by the year 2028. In response to the demand from major customers of large CMOS foundries, prominent CMOS foundries are actively integrating PIC-based optical connectivity into their technology offerings. Photonics on 300-mm technologies provide improved compatibility with the manufacturing processes of the electronic ASICs.

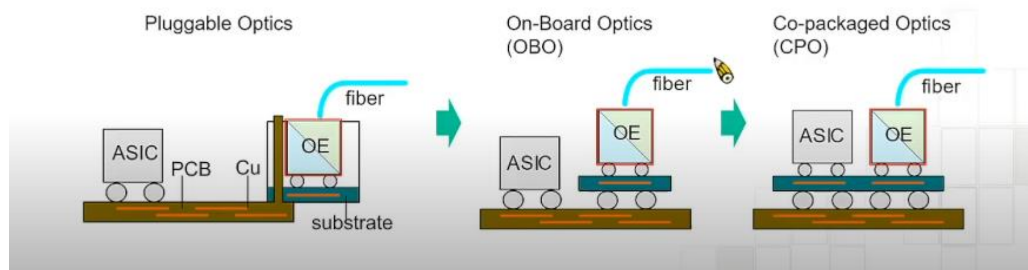


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Figure 11: Advancement in PIC-EIC integration, evolving from module-level and chip-on-package assembly to full co-integration on a single chip. Reproduced from "TSMC Packaging Technologies for Chiplets and 3D", Douglas Yu (TSMC)[24]

Growing demand for PIC-based solutions: The rapidly advancing integrated photonics technology offers versatility and a wide range of potential applications across various industries. Photonics21's in-depth whitepaper has comprehensively outlined the diverse applications of integrated photonics. Analysts predict a substantial increase in demand for PICs. These applications are made possible by the comprehensive integration of photonic functions on a chip, enabling innovations such as optical phased arrays for LIDARs, arrays of switches for quantum processors, and programmable photonic devices. Additionally, the technology's transparency window for photonic integrated circuits opens up possibilities for applications in biosensors, safety, and security. With the growing demands for optical connectivity and a diverse range of applications enabled by PICs, market analysts have projected demand for two 300-mm silicon photonics foundries by 2030 (Table 2).

Table 2: Demand for 300-mm fabs by 2030 as predicted by market analysts at a meeting of the Global Semiconductor Alliance, Munich 2024.

Node→	Logic	DRAM	NAND	Power	Photonic Integration
Capacity (KWPY)	480	1200	1600	530-670	280
Count (#)	6	8-12	3	1	2
Cost (B$)	125	130-200	30	5	4

Increasing scale of integration: Over recent years, there has been a significant increase in the number of building blocks on a single PIC, following a trend similar to Moore's Law for electronics (Figure 12). The PIC industry has achieved Very Large-Scale Integration (VLSI) for PICs with tens of thousands of optical functions on a chip. However, the current VLSI PICs are limited only to specific sets of building blocks. To fully unleash the potential of photonic integration for various applications such as high-speed transceivers, Lidars, optical computing, programmable photonics, and quantum signal processing, future VLSI PICs will require a broader mix of active and passive photonic building blocks. It will necessitate robust process control for enhanced yield. Photonics on 300-mm technologies offer a promising pathway to achieve large-scale integration with a richer mix of components.

[24]https://hc33.hotchips.org/assets/program/tutorials/2021%20HotChips%20TSMC%20Packaging%20Technologies%20for%20Chiplets%20and%203D_0819%20publish_public.pdf

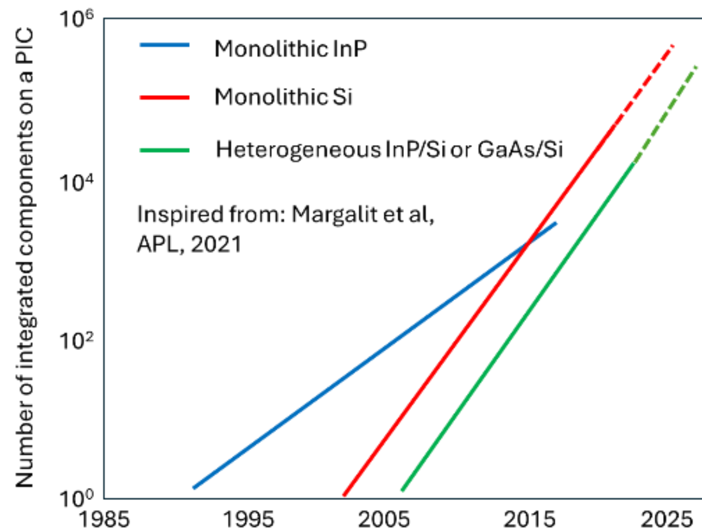
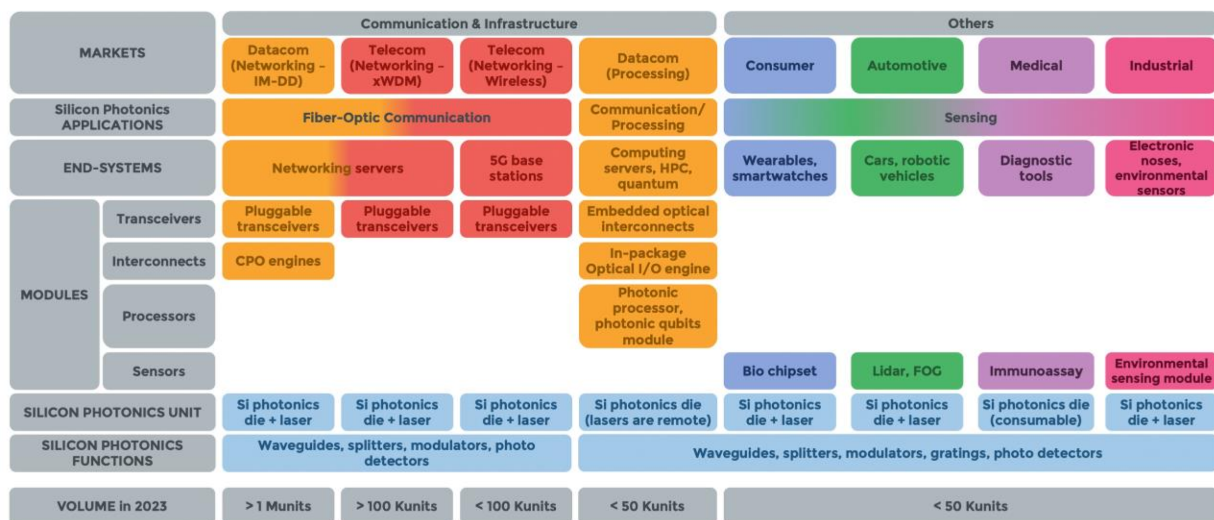


Figure 12: The revolution of the number of components integrated on a PIC chip for three integration platforms, including monolithic InP, monolithic Si and heterogenous InP and GaAs on Si. Inspired by Near Margalit, Chao Xiang, Steven M. Bowers, Alexis Bjorlin, Robert Blum, John E. Bowers; Perspective on the future of silicon photonics and electronics. Appl. Phys. Lett. 31 May 2021; 118 (22): 220501 [25].

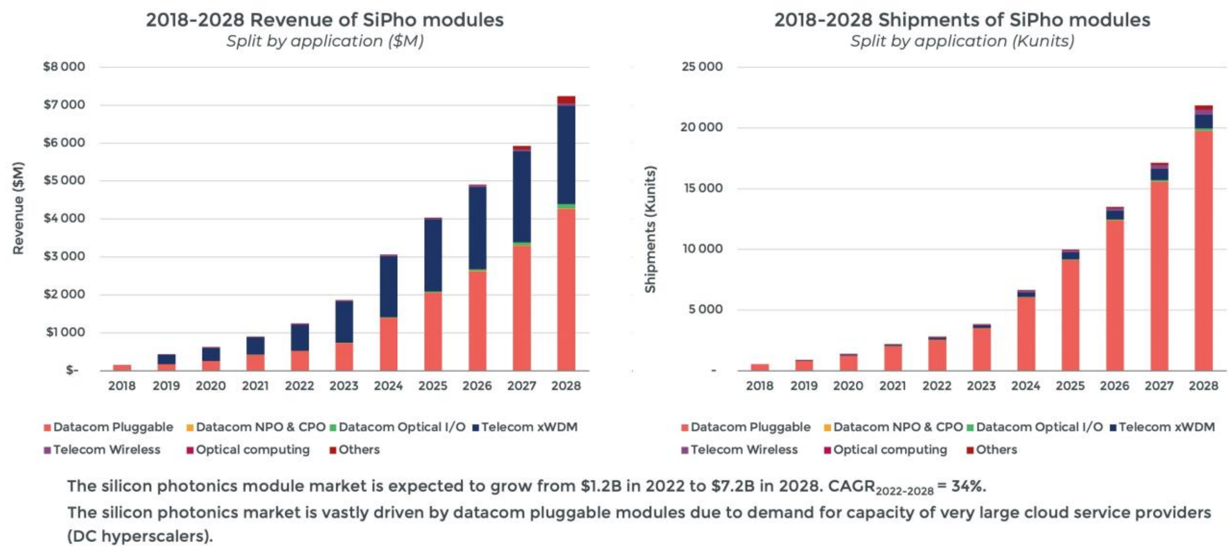
The segmentation of the growing number of PICS applications used by Yole Intelligence in its market analysis is shown in Figure 13*, and the expected revenues and shipment forecast are provided in* Figure 14.



[25] https://doi.org/10.1063/5.0050117

Figure 13: Segmentation used for Silicon Photonics application. Source: Silicon Photonics 2023, Yole Intelligence, November 2023.

2021 – 2028 SILICON PHOTONICS MARKET
– BY APPLICATION MODULES
Source: Silicon Photonics report, Yole Intelligence, 2023



www.yolegroup.com | ©Yole Intelligence 2024

Figure 14: Silicon Photonics market in units and revenue. Source: Silicon Photonics 2023, Yole Intelligence, November 2023.

7.6. SALES AND JOBS FORECASTS

According to the 2023 Yole Group report on silicon photonics, the market for PICs is set for substantial growth over the next decade, driven by increasing demand across various sectors. The market value is expected to rise from approximately €1.2 billion in 2022 to around €7.2 billion by 2028, reflecting a CAGR growth of about 34%. Significantly, the datacom segment is projected to lead this expansion, growing from €526 million to €4.4 billion, fuelled by escalating demand for high-speed data transmission and advanced networking solutions. The telecom sector is also anticipated to experience substantial growth, increasing from €710 million to €2.6 billion, driven by the deployment of next-generation optical networks and 5G infrastructure. Other applications like sensing, particularly in industrial automation and environmental monitoring, are expected to contribute significantly, with growth projected from €1 million to €184 million.

Furthermore, the anticipated growth underscores the critical need for advanced fabrication capabilities, such as 300-mm technology, to meet escalating demand in the growing PICs market. A European transition to larger wafer sizes will not only support higher throughput and economies of scale but also position European manufacturers to scale production to match the forecasted market expansion efficiently. This strategic investment in 300-mm technology will drive innovation and facilitate job creation, bolstering Europe's leadership in the global photonics industry.

In terms of jobs, the photonics sector is forecasted to create approximately 24,000 new jobs over the same period between 2022 and 2028, expanding from around 5,000 jobs in 2022 to approximately 29,000 jobs by 2028 (with an average earning of €250,000 per employee per revenue year). This growth will encompass a range of roles, including engineering, research and development, manufacturing, and operational support, highlighting the diverse opportunities within the industry. The projected job creation emphasises the significant impact silicon photonics can have on the European economy, fostering innovation and supporting a skilled workforce in a rapidly evolving technological landscape.

In 2028, for Europe, this will represent about 5,800 direct jobs with a market share of 20% as ambitioned by the Chips Act. This converts to more than 11,000 jobs in Europe, including indirect and induced jobs.

8. ANNEX A3 – 300 MM TOOLS

As described above in this document, one can easily identify several process steps which are necessary to produce usable components for PICs or imagers from a 300 mm wafer. Each of these process steps requires specific, dedicated, advanced tools that deliver the performance needed at this scale.

In order to clearly identify and state the challenges for each 300 mm tool, we propose here below a quick classification of the process steps to help sort the different corresponding tools:

- Epitaxy/deposition of materials with specific properties not used for CMOS process, such as:
  - Direct band gap semiconductors for photon absorption or emission at specific wavelength
  - Materials with a high-temperature coefficient of resistance, such as vanadium oxide (VOx) or amorphous silicon (a-Si) for micro-bolometers
  - Materials for polarisation-insensitive modulators
  - Dielectric materials for waveguides
  - Non-linear optical effect materials
- Lithography
- Etching
- Cleaning and surface preparation
- Wafer Level Testing

As mentioned above, all equipment and techniques related to wafer-to-wafer bonding, positioners, ion implanters, and micro-transfer printing can also be considered here to make the hyphenation between Si and III-V wafers possible.

8.1. EPITAXY

8.1.1. EPITAXY OVERVIEW

The epitaxy step consists of growing crystalline materials, typically III-V for photonics and new emerging oxides, such as $LiNbO_3$ considered as the "silicon of photonics", or STO/BTO), at the wafer scale, with atomic precision, onto a substrate. As mentioned above, when the InPoSi approach was introduced, the lattice mismatch between the substrate and the deposited materials should be controlled and mastered in order to avoid defects on the grown layer and guarantee maximal performance.

This step can be performed by several methods, like Molecular Beam Epitaxy - MBE, Metal-Organic Chemical Vapor Deposition – MOCVD - or other CVD techniques. MOCVD will not be detailed here since MOCVD tools are available for 300 mm wafers.

8.1.2. APPLICATIONS

MBE – Molecular Beam Epitaxy

MBE brings everything III-V, like InP or GaAs, and new materials, like STO/BTO, onto Si to open More-than-Moore possibilities or advanced optical properties.

Compared to other deposition or growth techniques, MBE features unique capabilities thanks to its ultra-high vacuum (UHV) conditions: high crystallinity, low growth temperature conditions enabling regrowth steps, and low defectivity.

An MBE tool is a “key technology enabler”: all the advantages mentioned above about cost, capacity, and performance are only virtual if the tool, which is at the first stage of the value chain, does not exist in the 300 mm version. This is especially true for all approaches involving direct deposition or full-scale wafer-to-wafer bonding, which are the most efficient in benefiting from these cost/performance/capacity advantages of 300 mm.

CBE - Chemical Beam Epitaxy and related techniques

MBE enables the development of high-quality and purity materials. However, it is not well adapted to the high temperatures required to deposit oxides and has relatively low growth rates. Chemical Beam Epitaxy is a promising growth technology in this respect.

Chemical Beam Epitaxy (CBE) (and related techniques, such as MOMBE, Metal-Organic Molecular Beam Epitaxy and GSMBE, Gas Source Molecular Beam Epitaxy)[26] were born in the 1980s from the merging of MBE (Molecular Beam Epitaxy) and CVD (Chemical Vapor Deposition), initially to deposit III-V semiconductor thin films. CBE takes from CVD the chemical reaction of a precursor molecule brought in the gas phase to react on the heated substrate to form the film, and from MBE, the molecular beam nature of the precursor flow, with line-of-sight molecule trajectories from the sources to the substrate. Applied to the III-V thin film growth, CBE gave excellent results, proving experimentally its advantages of (i) multi-element material controlled deposition and doping (for instance, deposition of the 4 element material GaAsInP [27]), (ii) high composition and thickness uniformity (for instance, 2% on 30 cm diameter deposition area [28]), (iii) high precursor conversion rate, (iv) high growth rates (typically, up to 10 microns per hours [29]) and (v) high reproducibility (typically, few % drift of the equipment over years [29]). The possibility of structuring the film during the growth with excimer laser irradiation was also proven [30], as well as the possibility of growing or etching selectively through shadow masks (selective area epitaxy [31]). Industrial tools were produced, and the technique was shown to enable the fabrication of integrated photonic devices (for instance, multi-wavelength laser [32]photo-diodes [33]). However, the CBE techniques did not manage at that time the expected breakthrough, although it was also developed for materials other than III-V semiconductors, including Si-containing materials (such as Si, Si_xGe_{1-x}, $FeSi_2$) and oxide materials (such as $LiTaO_3$ [34] or superconductive oxides for instance).

However, CBE tools dedicated to thin oxide film deposition are now available. They include an optimised gas distribution system to perform either rapid combinatorial complex material testing or highly homogeneous complex material deposition on substrate size between 150 and 450 mm.

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[26] Chemical Beam Epitaxy and Related Techniques | Wiley, Wiley.Com (n.d.). (accessed September 9, 2024)

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Research carried out on CBE demonstrated the high potentiality of the technique to grow high-quality layers, even epitaxial, for very critical materials becoming a must in photonics, such as $LiNbO_3$ [35] or $BaTiO_3$, or also promising preliminary results on $SrTiO_3$ layers [36]. The technique additionally offers the possibility of selective area deposition, either using shadow masks [37] or depositing on pre-patterned substrates [38], or irradiating locally with laser or electron beam [39].

These deposition systems are easily scalable to large deposition areas while still maintaining the deposit homogeneity (better than +/-1% on 450 mm). They can be used to deposit several elements either simultaneously or to build stacked layers. They are particularly promising in integrating devices that deposit directly in a structured way to avoid etching steps that are particularly complex on oxides and often detrimental to the surface quality.

In parallel to these chemical beam epitaxy systems, another "cousin" technology, labelled Hybrid-MBE, has developed, which mixes element sources and chemical precursor sources [40]. High-quality oxides have been deposited, with growth rates that are much larger than what is standardly obtained with MBE (up to 600 nm/h for $SrTiO_3$, for instance [41]).

CBE-related techniques have the potential to simultaneously address the present challenges of photonics scalability to 300 mm, integrating different materials within stacks and structuring small features with a high resolution [42,43]. The tools to develop the processes are available. Another interesting point is that they are particularly suitable for the new challenges open with the adoption of the new material class of epitaxial oxides, in addition to the most established ones of III-V semiconductors.

8.1.3. Market Characterisation

Epitaxy

- Performance
  - Performance expected from the market for these tools is highly related to the figures of merit that are expected for the wafers produced by the equipment; it can vary from one type of production to another, and FOM are not necessarily the same for imagers or PICs, for instance.
  - As a general rule, epitaxial UHV process, augmented with in situ instrumentation, will provide

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        - Low defectivity
        - Uniformity, stability, and reproducibility of the process
        - Controlled thickness for the deposited layer
    - A general figure of merit will also be the tool compatibility with SEMI rules to make it compatible with CMOS fabs
- Throughput: FOUP compatible
    - Exact throughput and yield will depend on the final devices considered;
    - The yield of an epitaxy batch should be a minimum of 85%
    - 24/24h, 7/7 operation
- Modularity
    - Not too modular; the tool, if well-designed, perfectly answers a given step of a given process.
- Connectivity to other tools: Cluster compatibility to connect with other techniques/tools
    - As a basis, the epitaxy tool would be a stand-alone tool
    - With a connectivity to EFEM
    - One machine = one process stage
    - The tool may include additional pre or post-process chambers but on a proprietary dedicated platform.
- Functionalities
    - Epitaxy controlled by advanced software
    - In situ instruments for real-time monitoring
    - Wafer deoxidation when necessary
    - Interfacing with SEMI Manufacturing Execution System
    - Warnings, auto securitisation, datalogger, communication process based on SEMI GEM 300

8.1.4. Market trends

Epitaxy is a niche market, and since it is only a single but vital process step, projections on a macroeconomic scale are not easily available in terms of CAGR.

The Yole Group report “Status of Compound Semiconductor Industry 2024” foresees a $100 million market for MBE in 2029, when the global market as of 2024 is estimated to be around $70 million [44].

Nevertheless, as the trend towards photonics and 300 mm is widely considered as being a strong driver for this market, 300 mm tools MBE tools sales will represent around ten installed units by 2029.

8.2. Wafer Level Testing

8.2.1. Wafer Level Testing Overview

In addition to the established use and reliability of conventional CMOS methods for growing and processing 300mm silicon wafers for photonic applications, the industry can build upon wafer-level handling and test architectures. The increased complexity of handling light has made electro-optical testing and wafer qualification crucial steps for identifying defects before devices are integrated into final products, where yield issues can be extremely costly.

Testing photonic integrated circuits (PICs) is highly complex due to the wide range of product types, mechanical configurations, and the need to handle light simultaneously. PICs can consist of various silicon-based submodules

[44] https://www.yolegroup.com/player-interviews/mbe-becomes-critical-for-high-quality-gaas-and-gan-epitaxy-an-interview-with-veeco/

such as optical inputs/outputs, ring resonators, modulators, and waveguides. These components can be tested by upgrading existing infrastructure to accommodate new optical requirements, but this introduces new challenges. Precision alignment of optical fibres for coupling light in and out of a PIC, along with intricate electro-optical testing sequences, is essential to assess optical performance, such as wavelength and polarisation-dependent losses, while also probing electrical system parameters.

8.2.2. Applications

A fully functional automated wafer-level tester (WLT) provides foundries and outsourced semiconductor assembly and test (OSAT) suppliers with streamlined and efficient ways to qualify wafers early in the process. WLT systems enable users to correlate test results with end-of-line data and facilitate chip traceability, aiding in the fine-tuning of process and quality metrics.

Electro-optical testing methodologies can generally be divided into three main categories:

1. **Passive optical testing**: Used for testing components that do not require electrical excitation, such as waveguides and optical couplers.
2. **Low-speed or DC electro-optical testing**: Used for fundamental performance testing of lasers, photo-diodes, ring resonators, modulator spectral validation, and more.
3. **High-speed electro-optical testing**: Used for testing fully functional hybrid PICs, modulators, ring resonator performance, and more.

8.2.3. Market Characterisation

WLT product key capabilities are:

- Autoloading and unloading of up to 300mm-diameter wafers, with an interface to foundry robotic systems.
- Six-axis positioners (east/west) to enable optical measurements of common mechanical configurations, with the ability to modify for other configurations as needed.
- Simple interface for attaching fibre array units (FAUs) to optical positioners.
- Positioners (north/south) for electrical measurements using discrete parametric probes, with an optional probe-card positioner interface for additional contacts.
- Thermal chuck to enable temperature testing and the testing of broken wafers.
- Auxiliary (AUX) chucks for:
  - High-frequency calibration of parametric probes or probe card
  - Probe and probe card cleaning
  - In-situ FAU validation
- Test equipment storage and fibre organisation

Key factors influencing market growth include:

- **Technology Miniaturisation:** Shrinking transistor sizes (e.g., from 7nm to 3nm nodes) demand more precise and comprehensive testing.
- **Increased Complexity:** More advanced devices, such as system-on-chip (SoC) designs, require additional test coverage and validation before packaging.
- **Cost Efficiency:** Wafer-level testing reduces manufacturing costs by identifying defective dies early, minimising wasted packaging on faulty devices.

8.2.4. Market trends

Wafer-level testing (WLT) plays a critical role in the semiconductor manufacturing process, ensuring that individual dies are functional before being diced from the wafer. This market has seen significant growth due to increasing demand for advanced semiconductor devices driven by applications in AI, 5G, automotive electronics, and IoT. As per the current market research conducted by the CMI Team, the global Semiconductor Testing market is expected to record a CAGR of 7% from 2023 to 2032. In 2022, the market size was projected to reach a valuation of $34.7 billion. By 2032, the valuation is anticipated to reach $54.2 billion.[45]

The following bar chart (Figure 15) breaks down the WLT market by major regions:

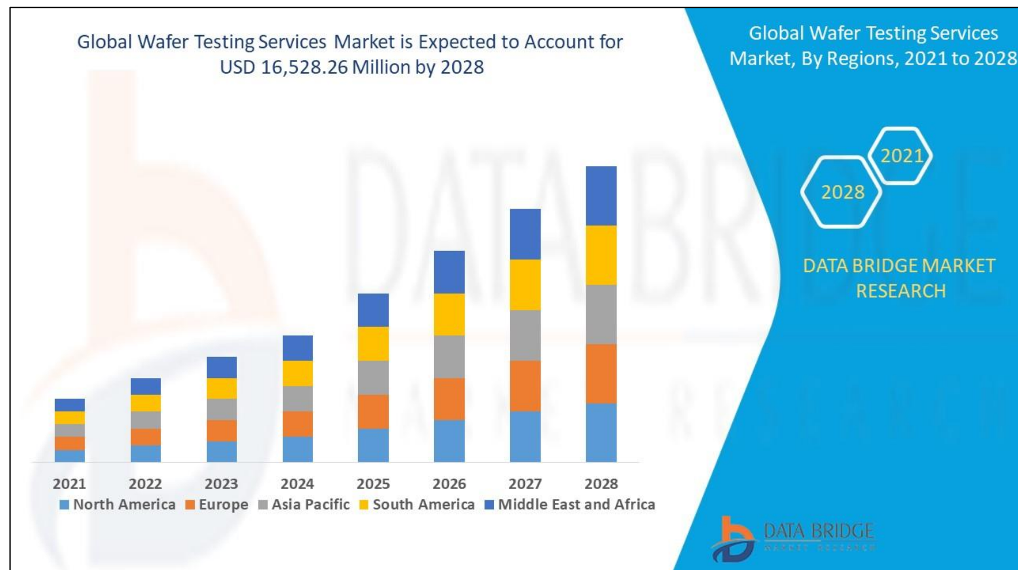

Figure 15: Global wafer testing services market [46]

8.3. Sales and Job Forecast for 300 mm Tools

The semiconductor value chain includes seven differentiated activities, from pre-competitive research to design, front-end wafer fabrication, back-end assembly, packaging & test, electronic design automation & core IP, equipment & tools and materials. The equipment & tools activity is the category of interest for evaluating the 300 mm tool market for the micro-bolometer and PICs products described in annexes A1 and A2. It represents 11% of the value of semiconductor products[47]. For micro-bolometer and PICs products, the market is estimated to be € 8.8 billion in 2028/29. The equipment and tools market can thus be evaluated at around € 0.97 billion.

Within this market, the tools described in Annex A3 are in the Deposition and Test & Related Equipment categories. Figure 16 shows the breakdown of the tools required to manufacture semiconductor products[47], which represent about 28% of the total semiconductor tool market.

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[45] https://www.custommarketinsights.com/report/semiconductor-testing-market/

[46] https://www.databridgemarketresearch.com/reports/global-wafer-testing-services-market

[47] https://www.semiconductors.org/wp-content/uploads/2021/05/BCG-x-SIA-Strengthening-the-Global-Semiconductor-Value-Chain-April-2021_1.pdf

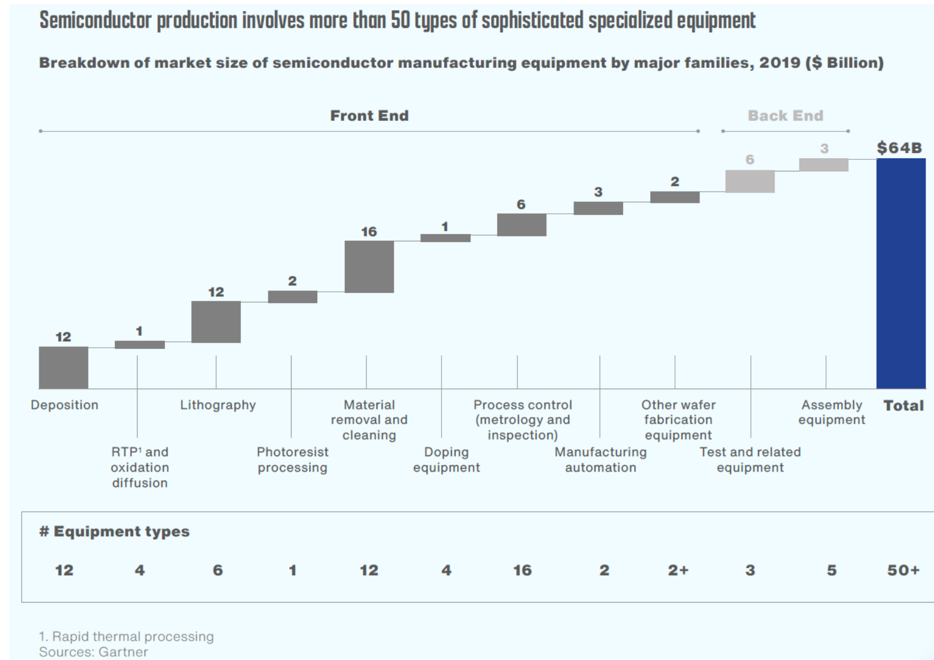

Figure 16: Breakdown of market size of semiconductor manufacturing equipment by major process families. Extracted from BCG/SIA report "Strengthening the Global Semiconductor Supply Chain in an Uncertain Era", April 2021[47].

Considering the consolidated market of € 0.97 billion for micro-bolometer imagers and PICs tools, we can estimate the combined deposition and wafer level test market for these two categories of photonics products to be worth €270 million in 2028/29. For Europe, considering a 20% market share as ambitioned by the Chips Act, this will represent about € 54 million in sales and 220 direct jobs. This converts to more than 400 jobs in Europe, including indirect and induced jobs.